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# MS-7276 uATX Version: 20

**CPU:** Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe family processors in LGA775 Package.

## System Chipset:

Intel BroadwaterG965/Q965 (North Bridge)  
Intel ICH8DO / DH (South Bridge)

## On Board Device:

BIOS -- SPI Flash 16M  
Azalia Codec -- ALC888  
LPC Super I/O -- W83627DHG  
LAN -- NINEVEH/EKRON  
CLOCK Gen -- ICS 9LPR502 (56pin)  
1394 Controller -- VT6307 (2-port)  
Hi-USB to PATA Bridge -- JM20335

## Main Memory:

Dual-channel DDR-II \* 4 (Max 4GB)


## Expansion Slots:

PCI EXPRESS X16 SLOT \*1  
PCI EXPRESS X1 SLOT \* 1  
PCI SLOT \* 2

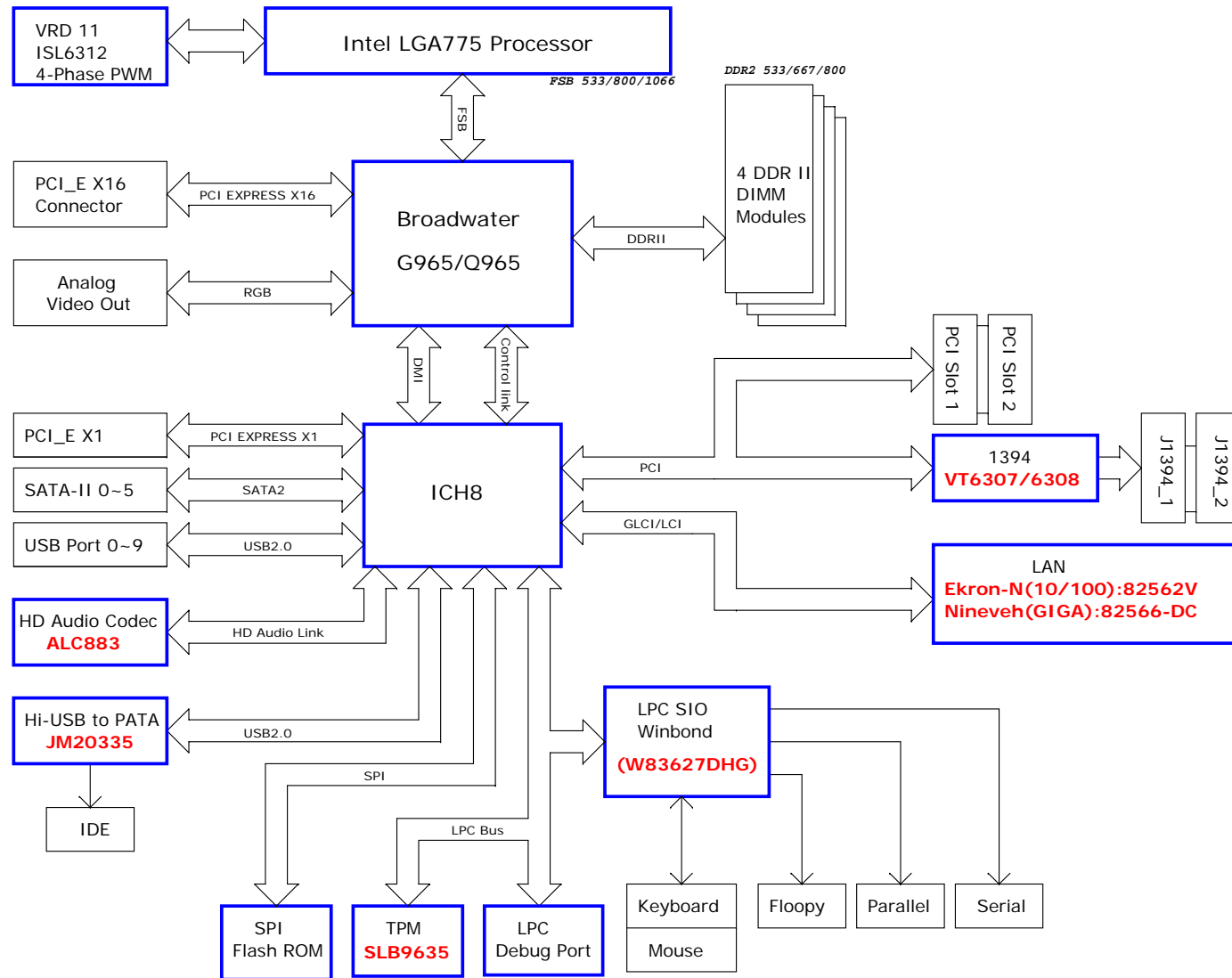
## Intersil PWM:

Controller: Intersil ISL6312 (4 Phases)  
Driver: Intersil ISL6612

Option	Function	Orcad Configure	BOM
STD	Broadwater/ICH8/W83627DHG/ALC883/82566DM/USB to IDE	cfg-STD	

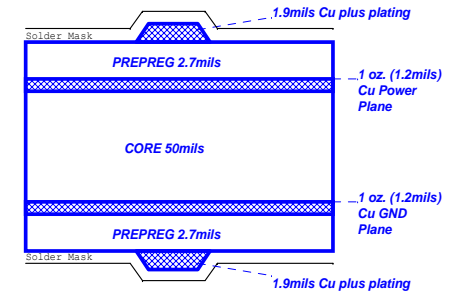
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# Block Diagram



## Board Stack-up

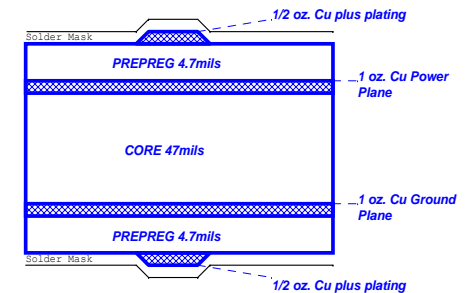
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils  
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15  
 SATA - 95ohm : 15/4/8/4/15  
 LAN - 100ohm : 15/4/8/4/15  
 PCIE - 95ohm : 15/4/8/4/15  
 IEEE1394 - 110ohm : 15/4/9/4/15  
 IDE : 15/4/8/4/15

## Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils  
 IEEE1394 - 110ohm Top : 5/7/5  
 PCIE, LAN, SATA - 100ohm Top : 5/6/5  
 USB2.0 - 90ohm Top : 7.5/7.5/7.5

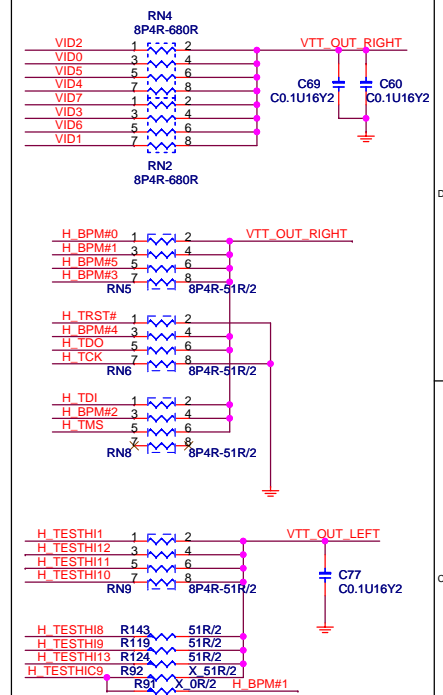
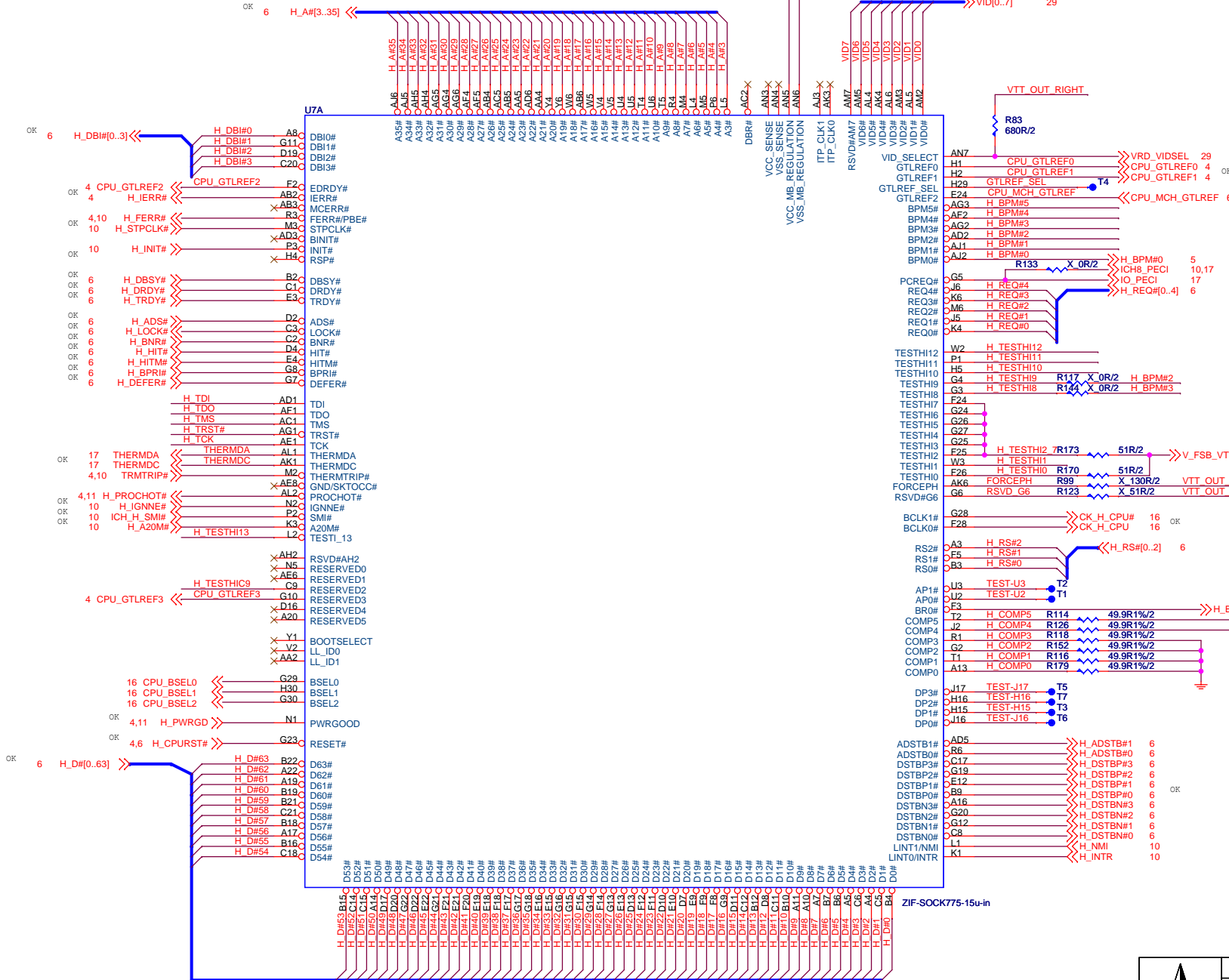


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## CPU SIGNAL BLOCK

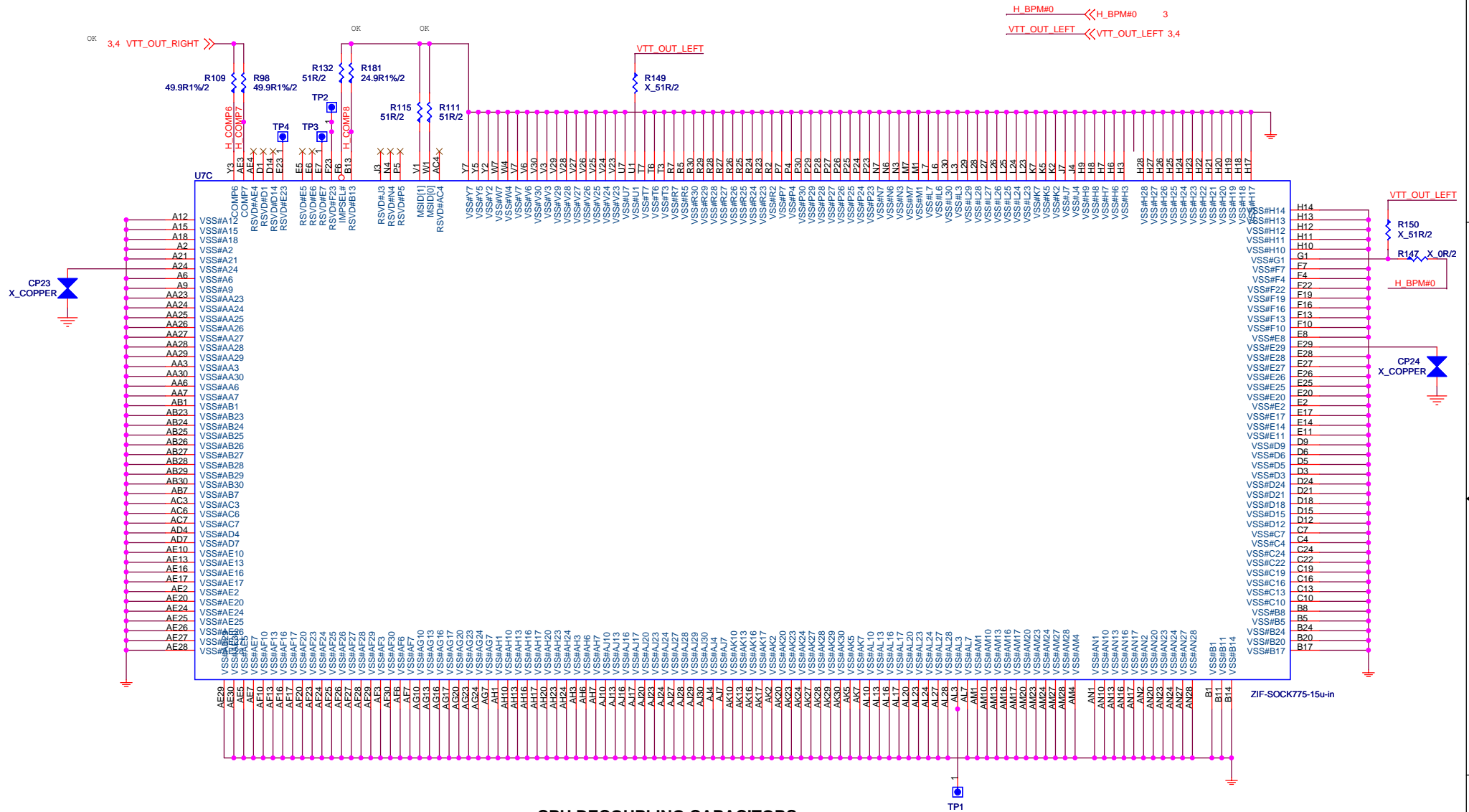


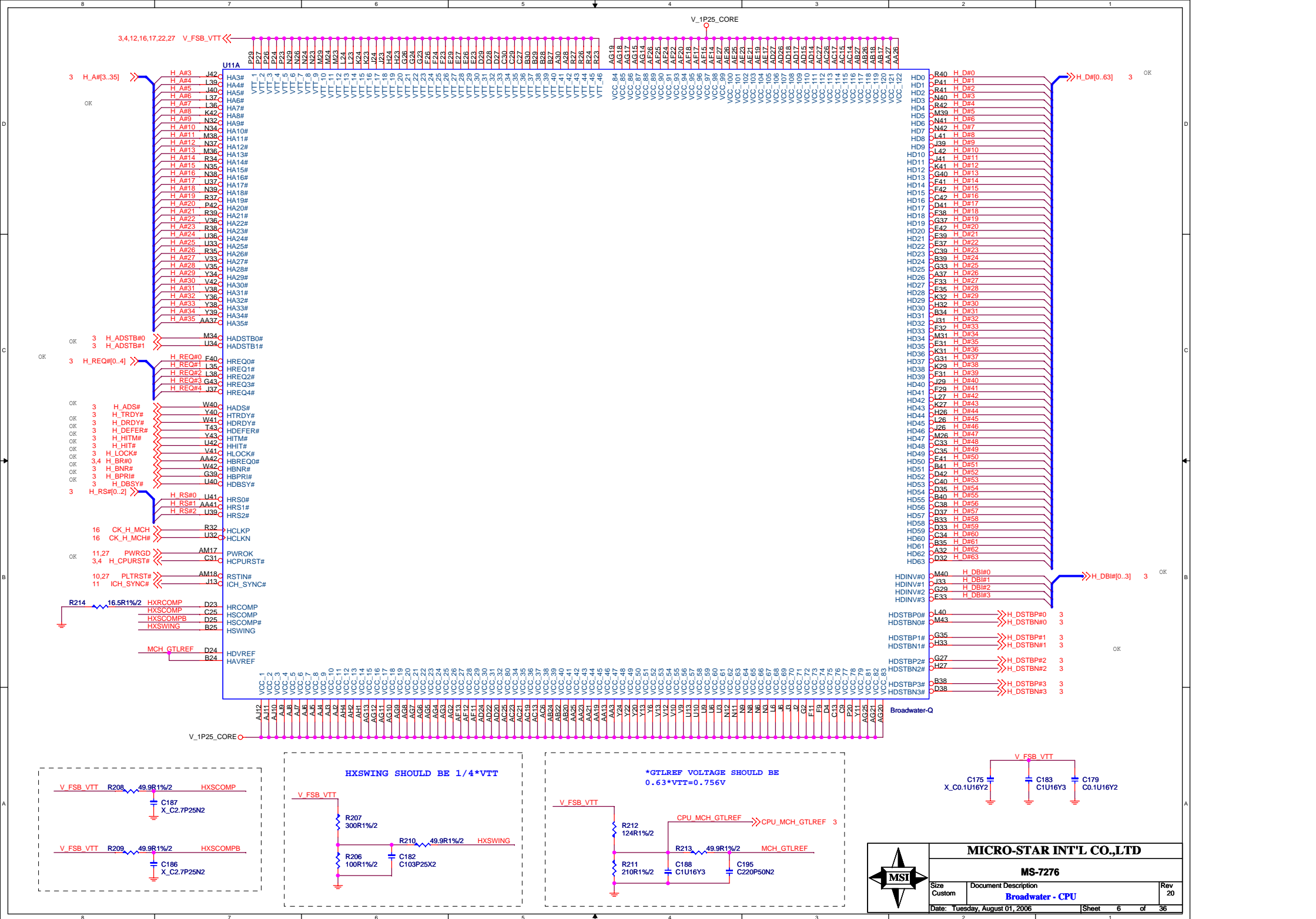
**MICRO-STAR INT'L CO.,LTD**

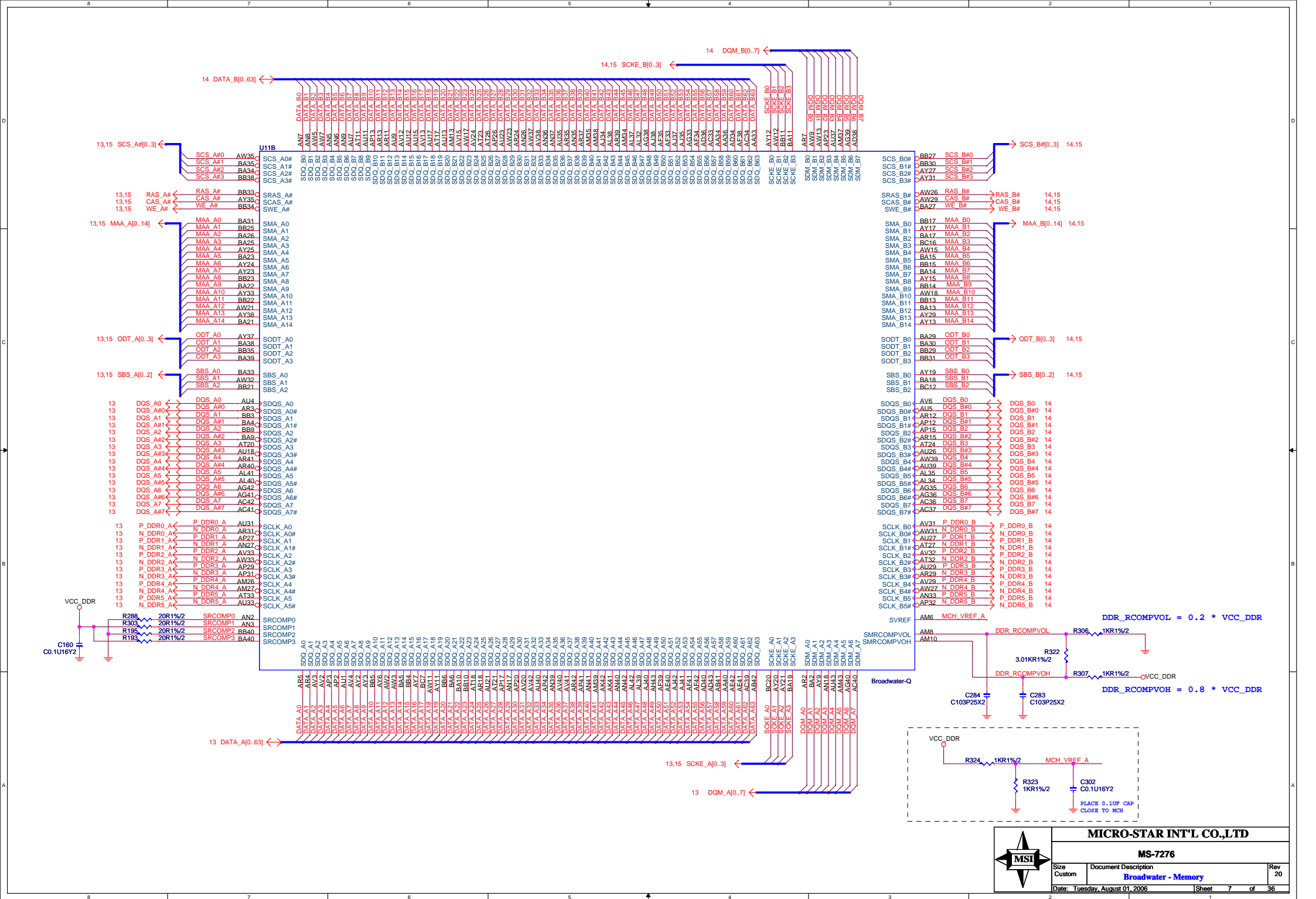
MS-7276

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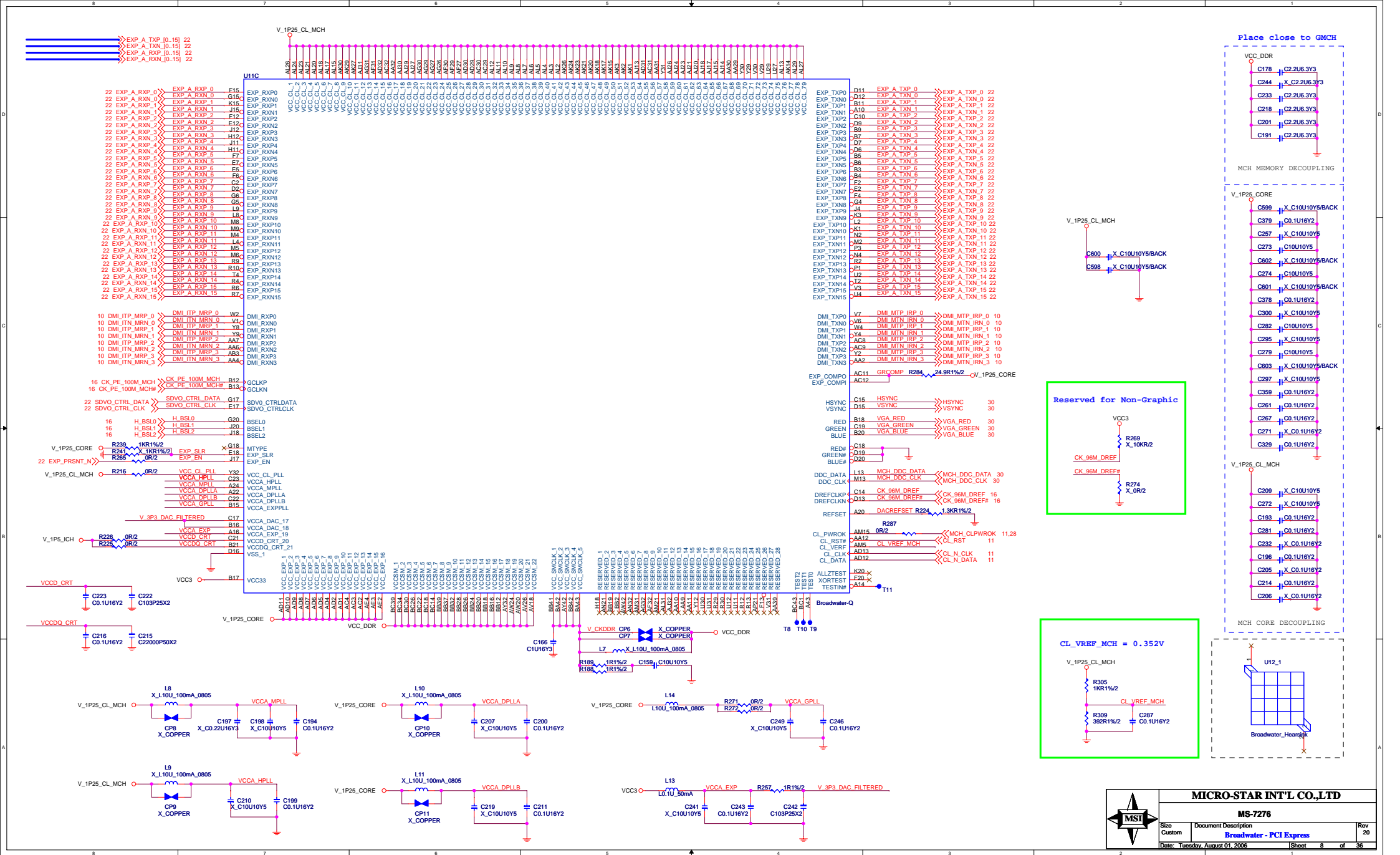








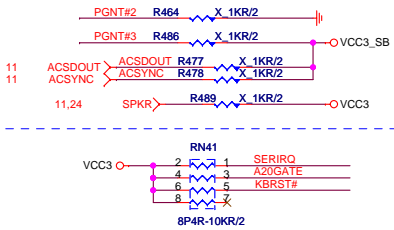




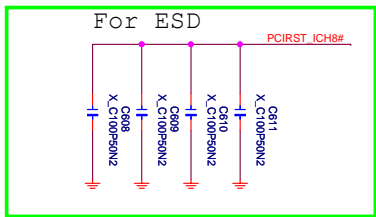




ICH8 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRM/ LAN100_SLP	EN	DIS	INT VRM (VccSus1_05,1_5,VccCL1_5) (VccLAN1_05,VccCL1_05)
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/ PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

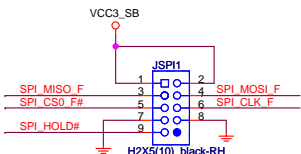


BOOT SELECT STRAPS			
BOOT DEVICE	GNT0	SPI_CS1#	
FWH	1	1	
SPI	0	X	
PCI	1	0	



### SPI DEBUG PROT

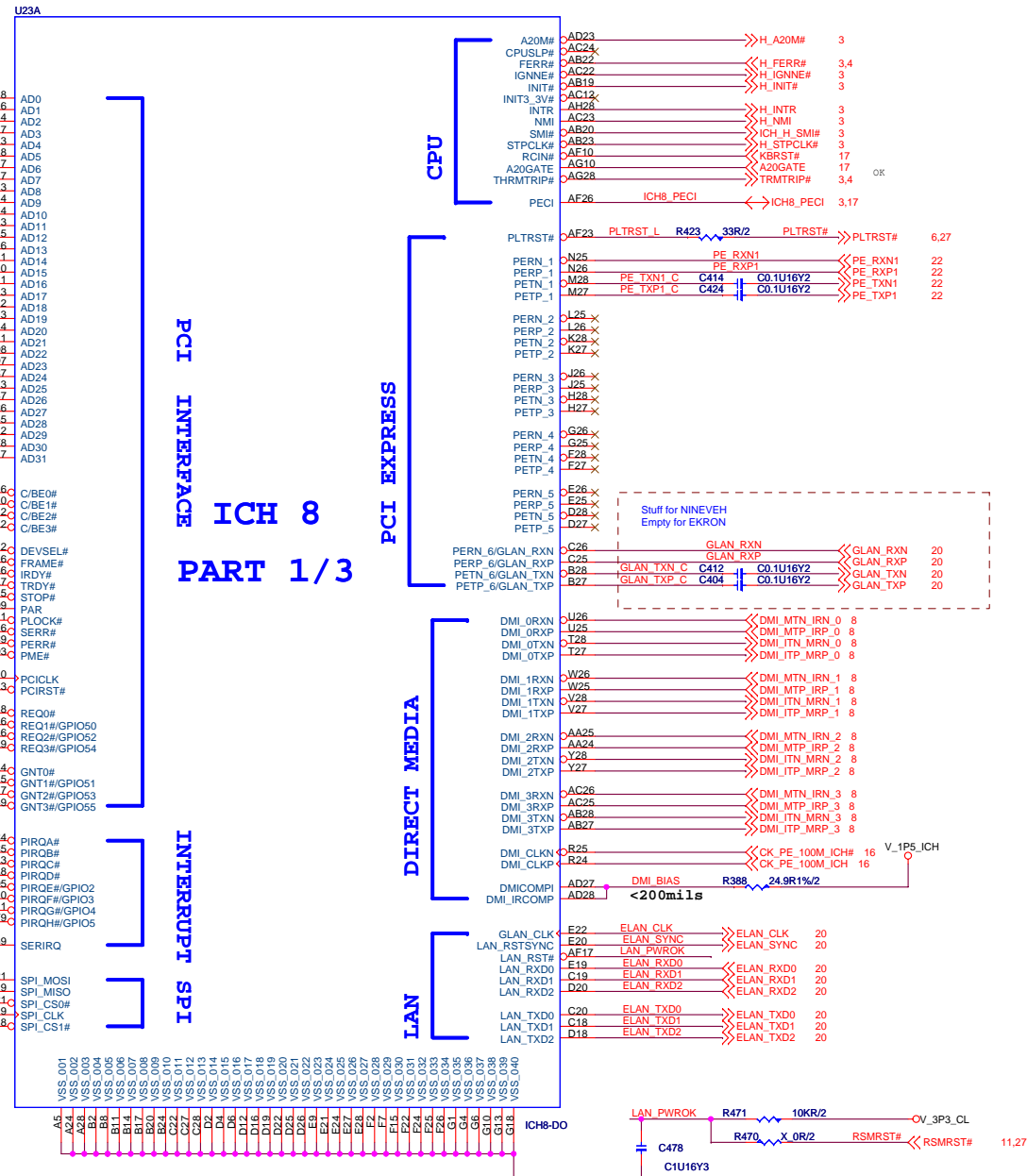
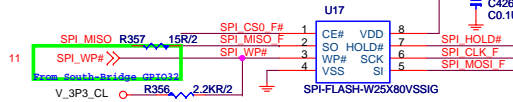
Place close to SPI ROM



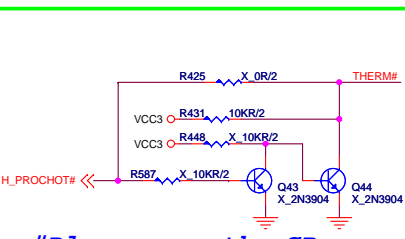
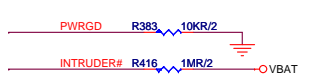
Part Number : N31-2051451-H06

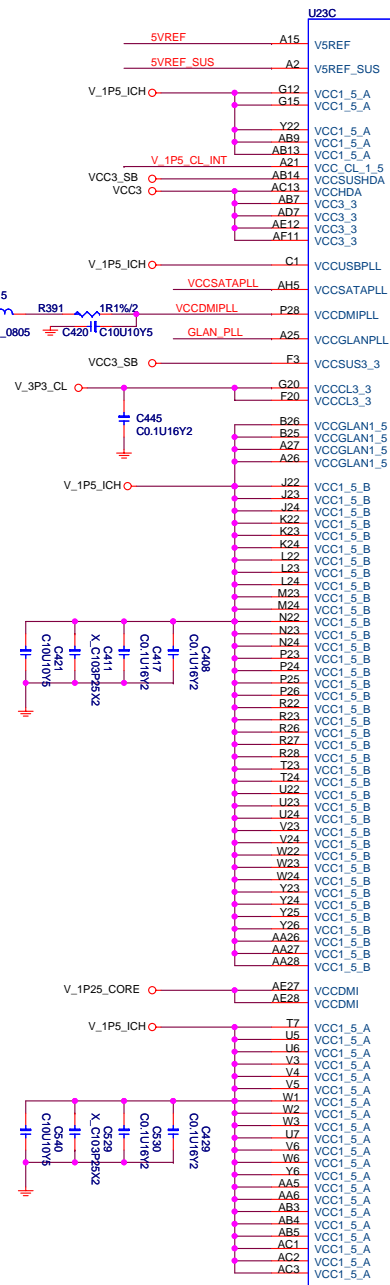
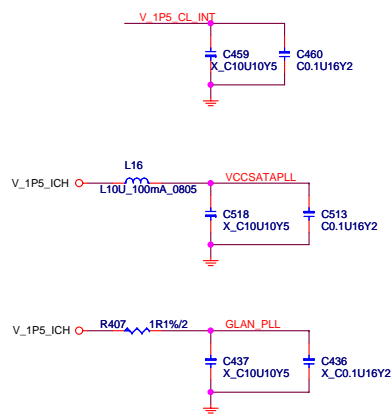
### SPI FLASH ROM

Place close to SB.



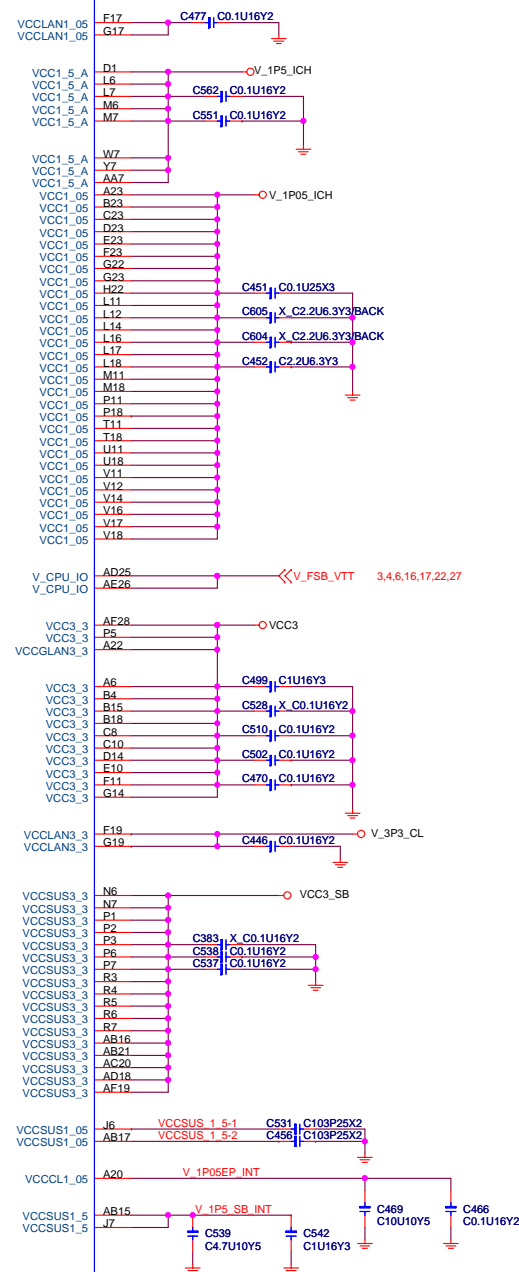
Trace length is less than 3inchs to ICH8.





ICH 8

PART 3/3



ICH8-DO



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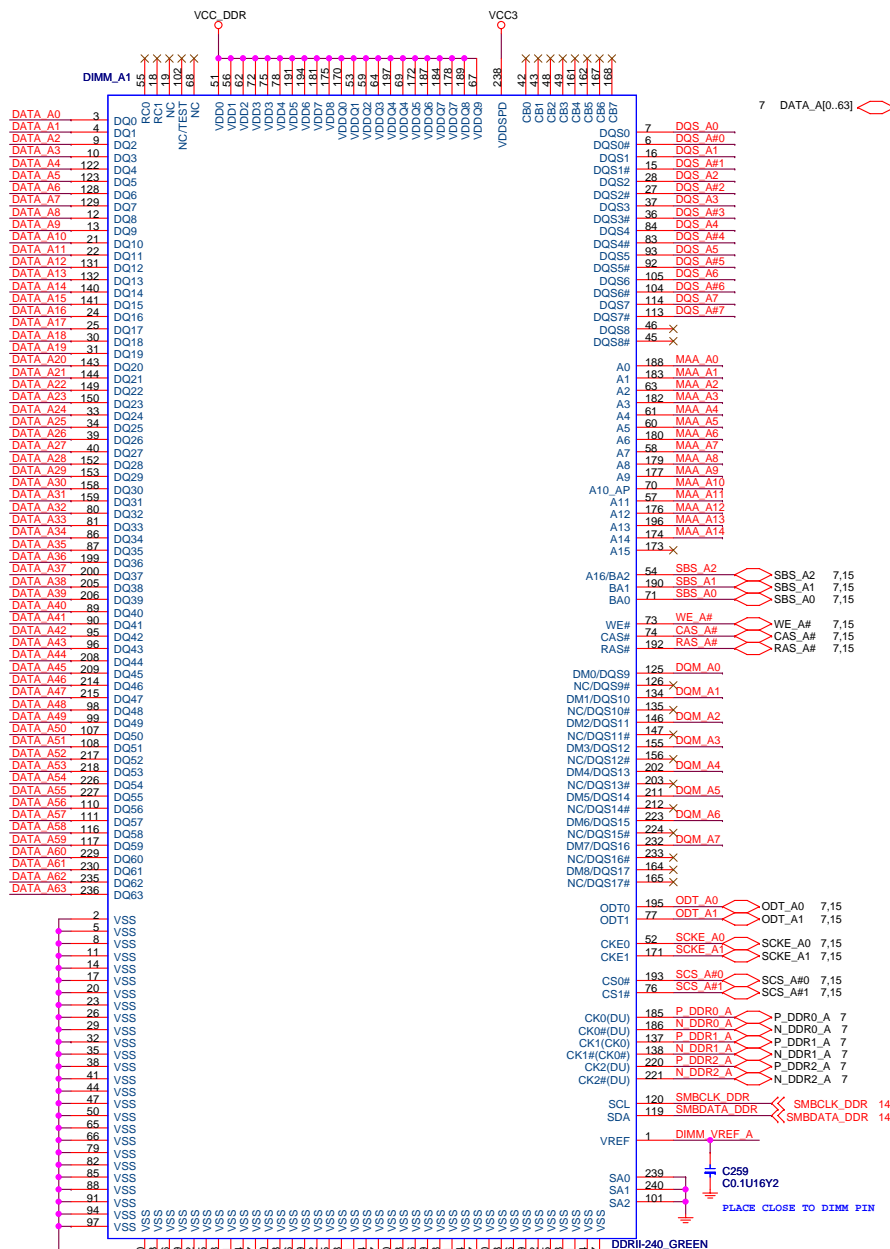
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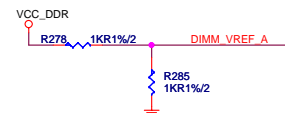
Custom **ICH8. POWER**

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Obtaining	10	-1	20
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## DDRII DIMM\_A1



ADDRESS: 000  
0xA0



## DDRII DIMM\_A2



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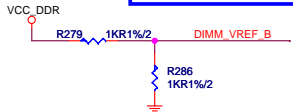
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## DDRII DIMM\_B1

ADDRESS: 010  
0xA4



SMBCLK\_DDR  
SMBDATA\_DDR



## DDRII DIMM\_B2

ADDRESS: 011  
0xA6



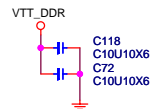
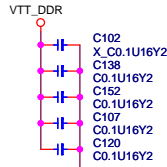
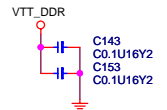
MICRO-STAR INT'L CO.,LTD

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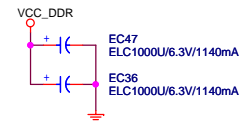
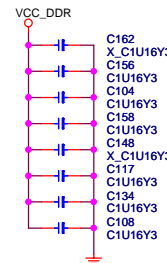
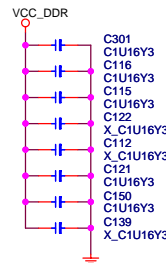
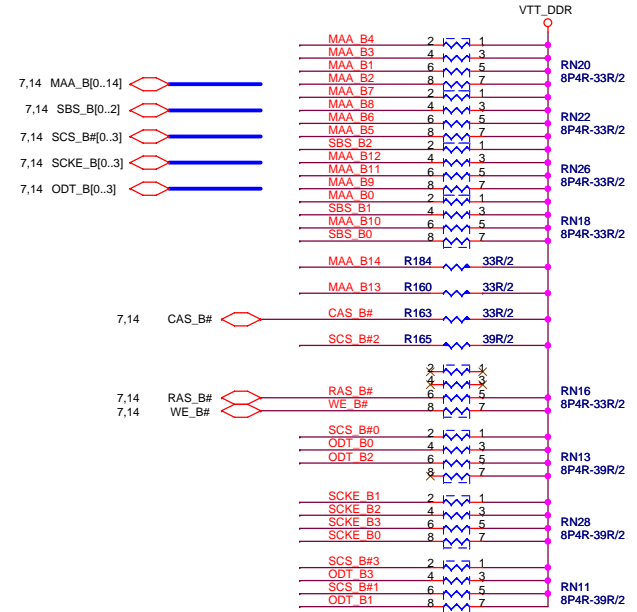
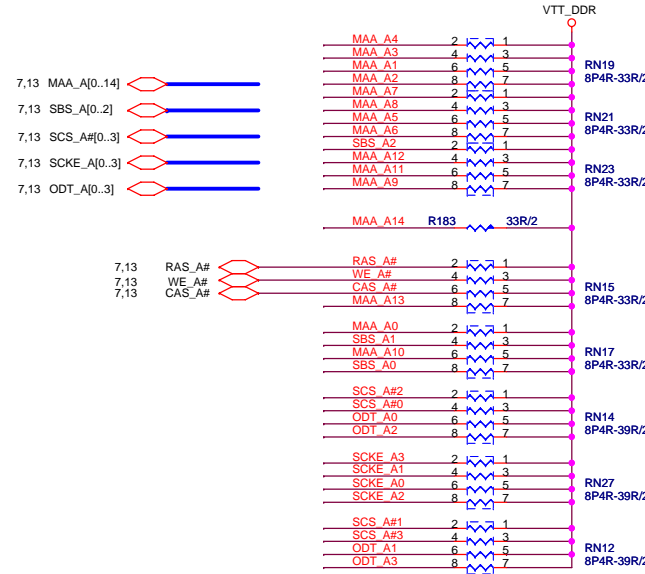
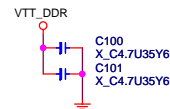
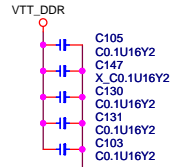
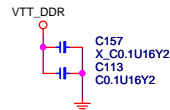
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CHANNEL A V<sub>SM\_VTT</sub>  
DECOUPLING CAPS



CHANNEL B V<sub>SM\_VTT</sub>  
DECOUPLING CAPS



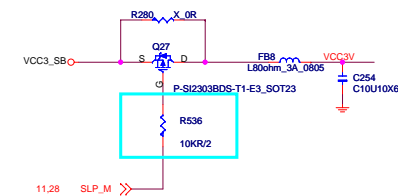
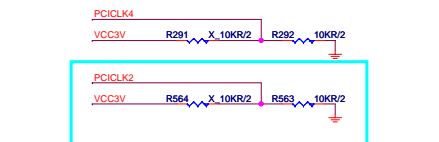
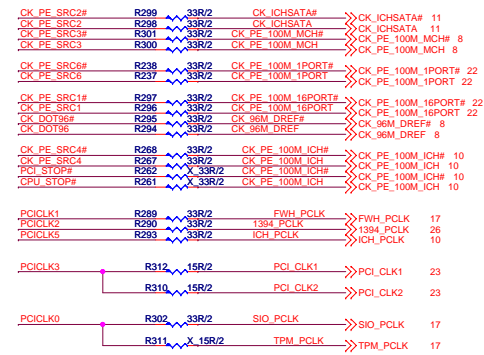
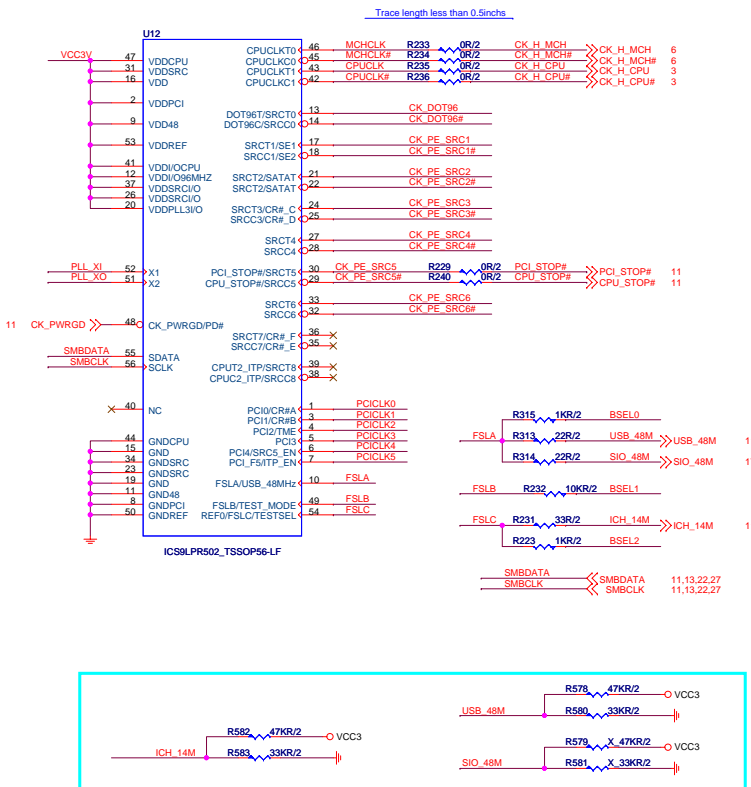
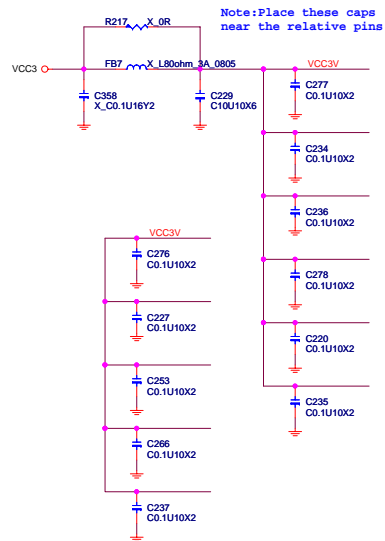
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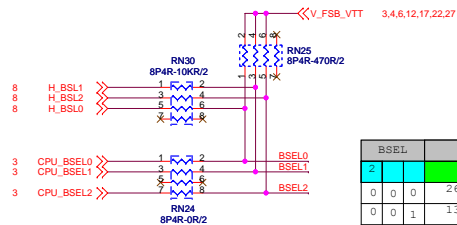
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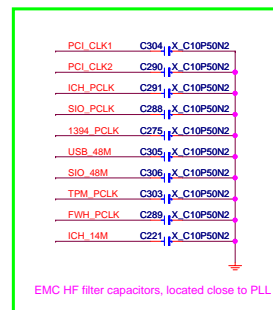
## Clock Generator - ICS9LPR502



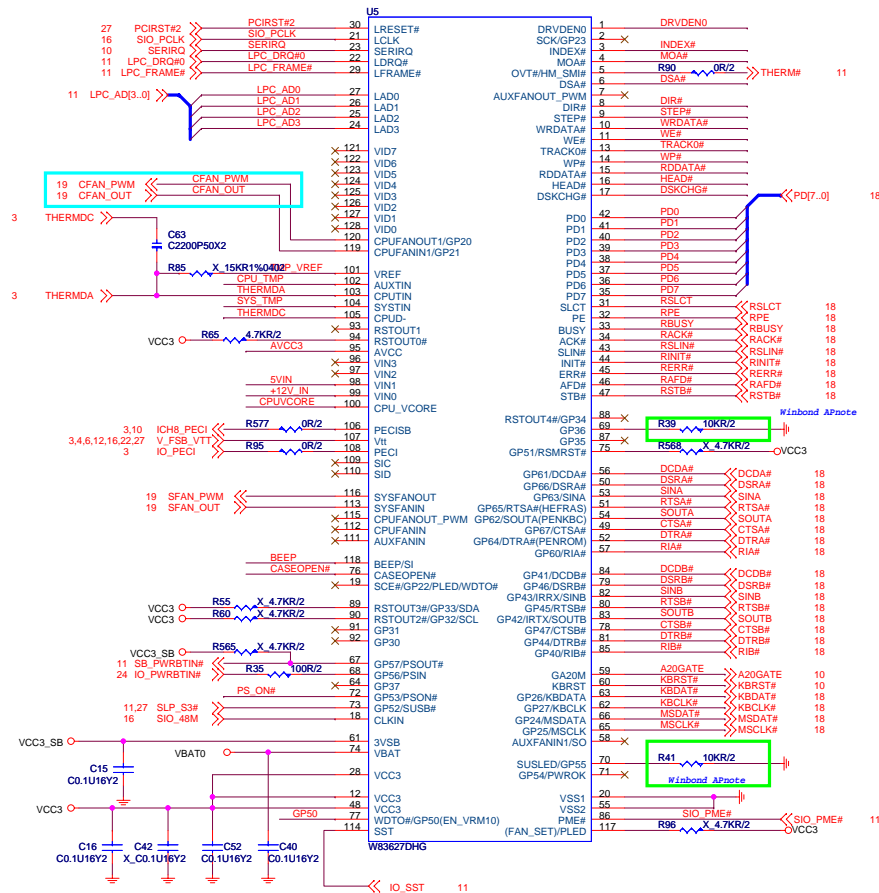
### BSEL[0..2] Level Shift



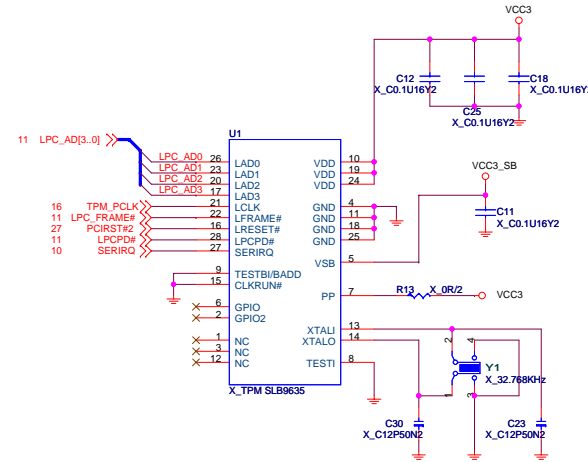
BSEL			TABLE
2			
0	0	0	266 MHz (1066)
0	0	1	133 MHz (533)
0	1	0	200 MHz (800)



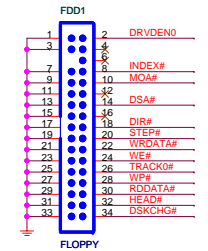
## LPC SUPER I/O W83627DHG



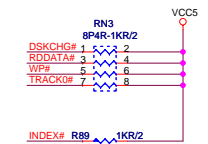
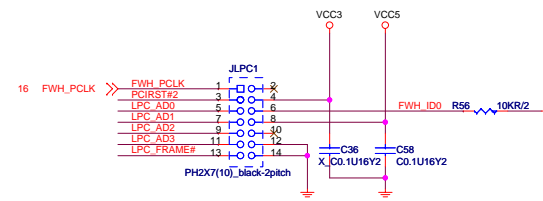
## TPM - Security Controller



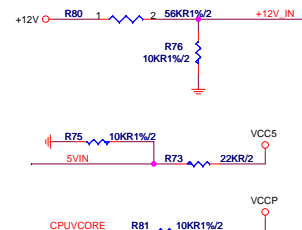
## FLOPPY CONNECTOR



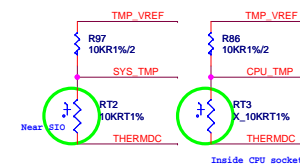
## LPC Debug Port



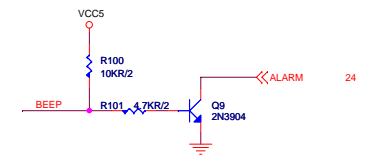
## Voltage Detect



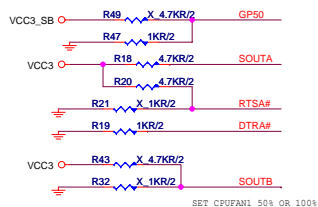
## Temperature Sensor



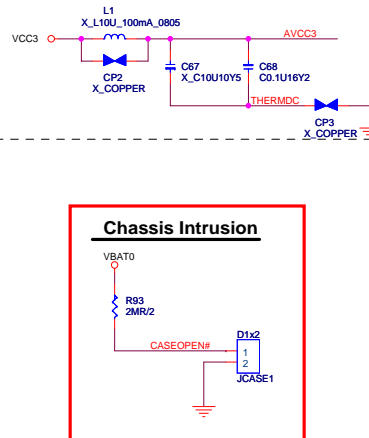
## Beep



## LPC I/O STRAPPING RESISTOR

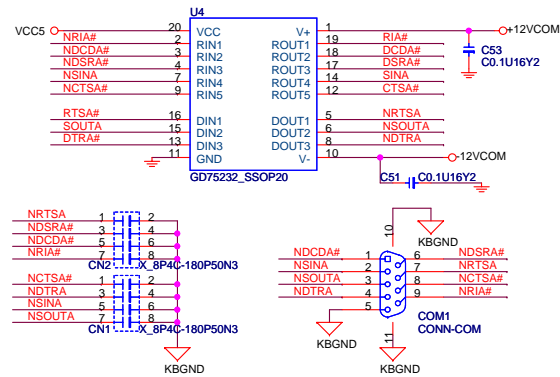
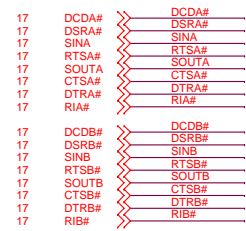


## Chassis Intrusion

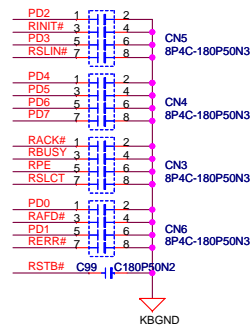
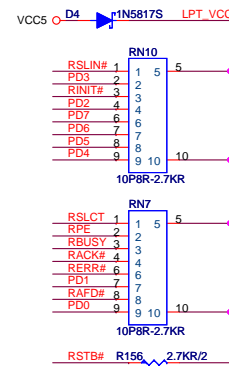
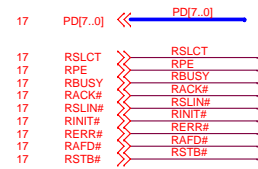
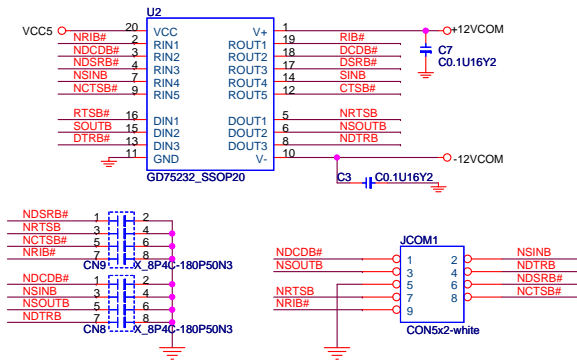


RTSA#	L: CFAD-2E	H: CFAD-4E
GP50	L: TTL LEVEL	H: VRM10 LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRA#	L: DISABLE SPI	H: ENABLE SPI

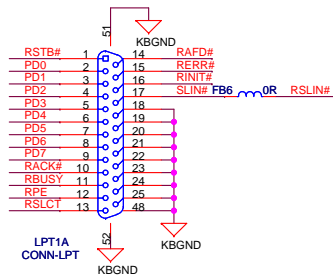
## SERIAL PORT 1



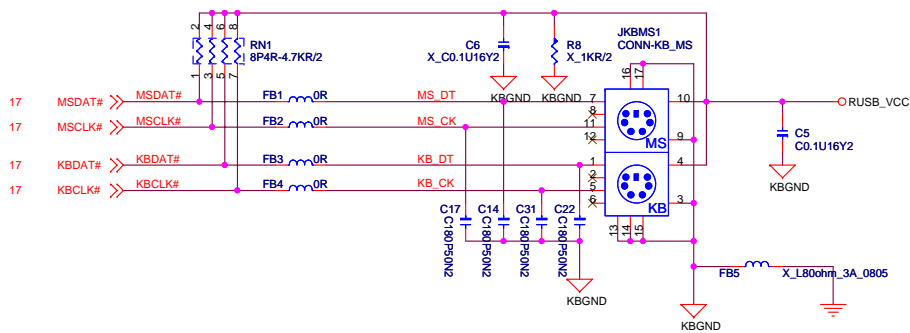
## SERIAL PORT 2



## PARALLAL PORT

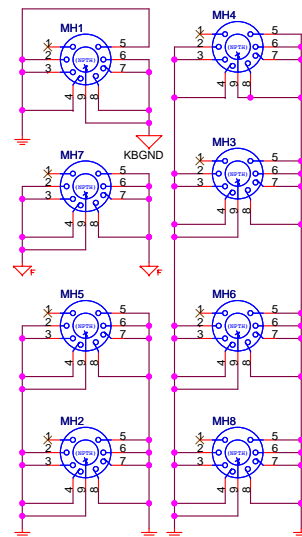


## PS2 KEYBOARD & MOUSE CONNECTOR

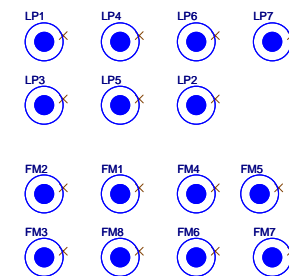


layout 蛸碑口 KBGND鶴GNDと妻菴 蛸 ?50mil腔料蓋眈窠

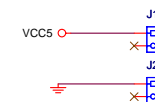
## Mounting Holes



### Optics Orientation Holes



## Simulation

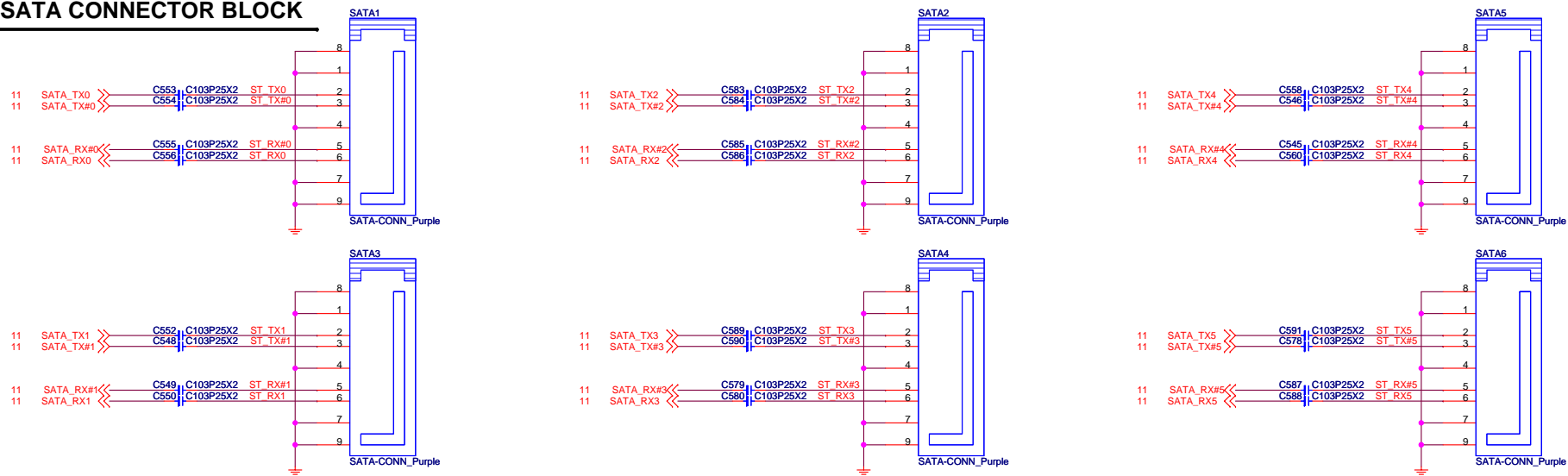


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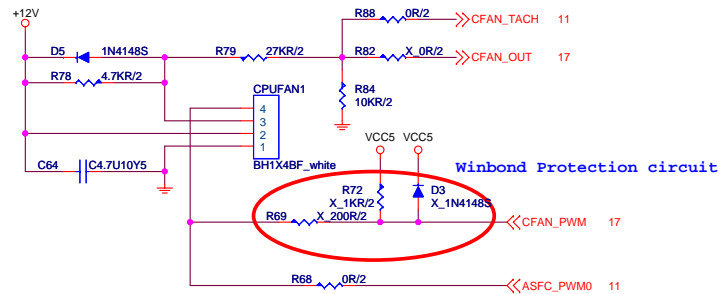
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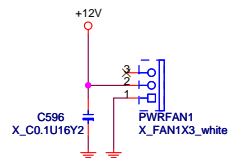
## SATA CONNECTOR BLOCK



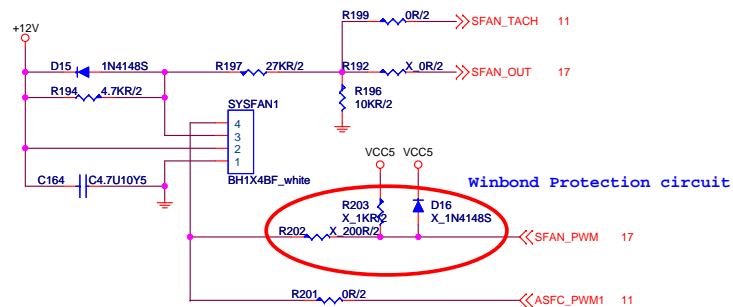
## CPU FAN



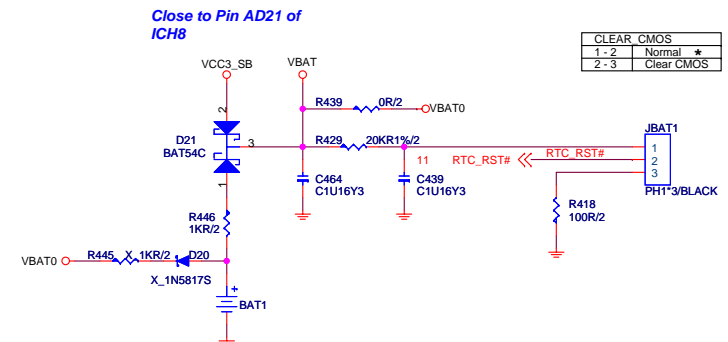
## POWER FAN



## SYSTEM FAN



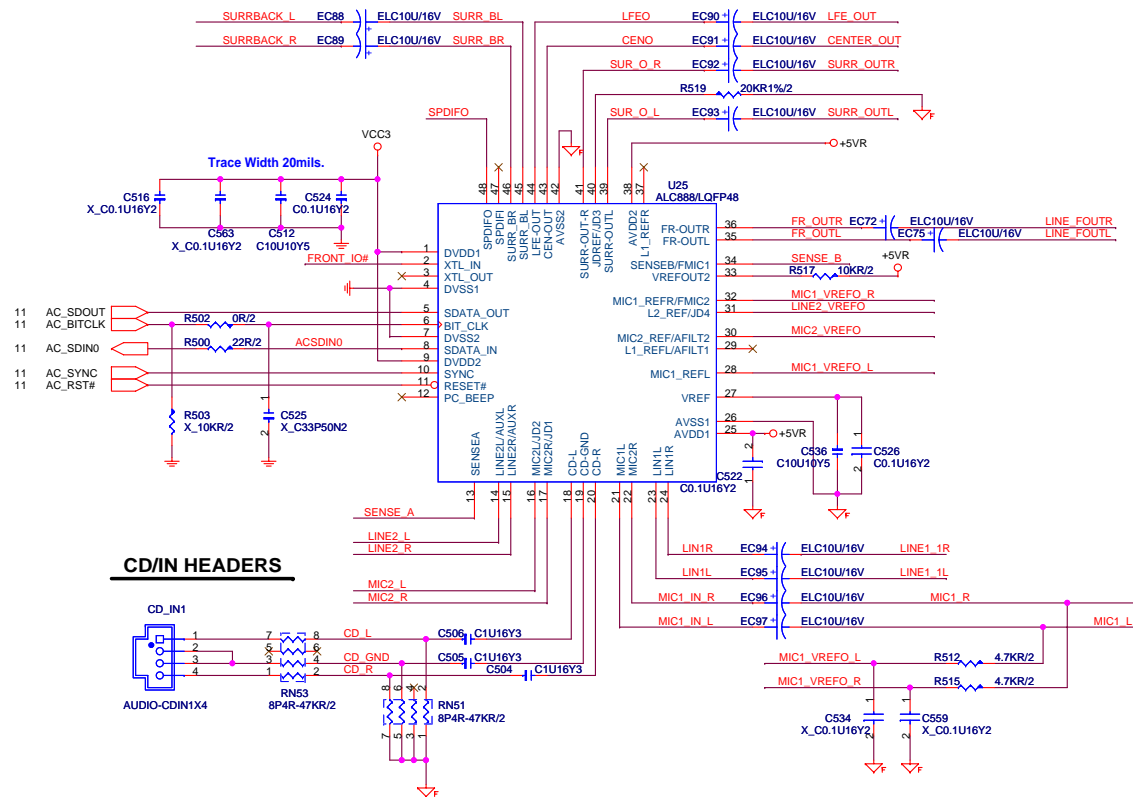
## RTC BLOCK



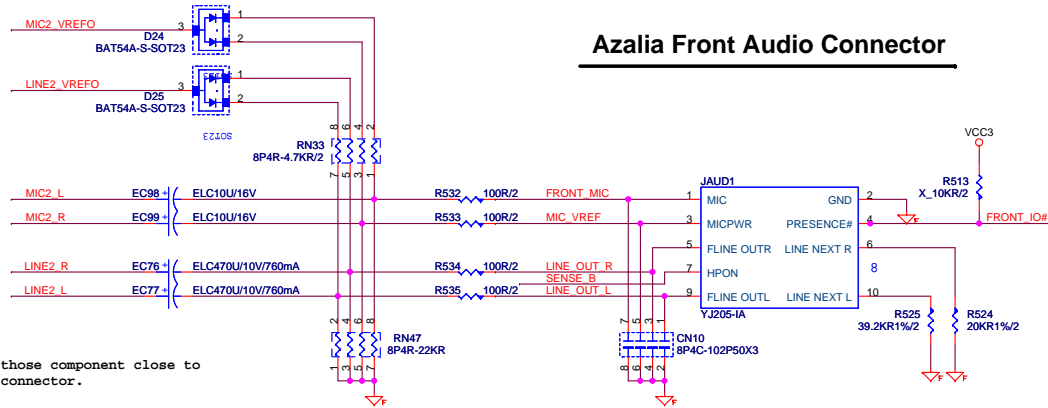
CLEAR CMOS		
1 - 2	Normal	★
2 - 3	Clear CMOS	



## ALC888 CODEC

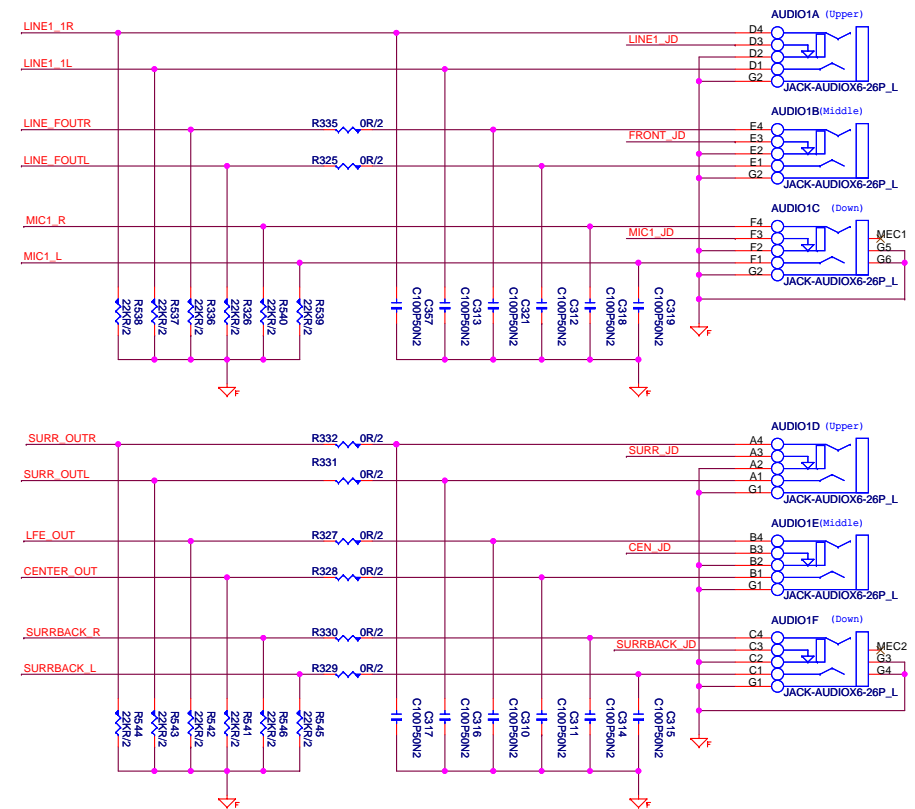


## Azalia Front Audio Connector

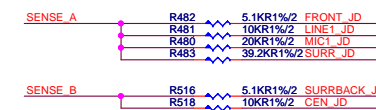


Place those component close to  
audio connector.

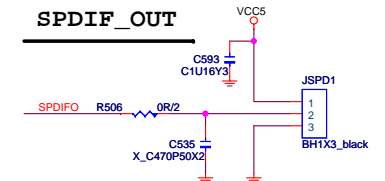
ALC883 JACK



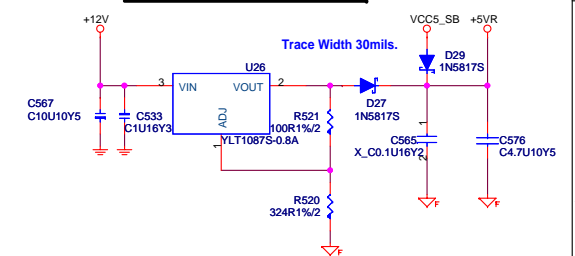
ALC883 JACK DETECT



## SPDIF\_OUT



## AUDIO CODE REGULATORS



**MICRO-STAR INT'L CO.,LTD**

MS-7276

Size  
Custom

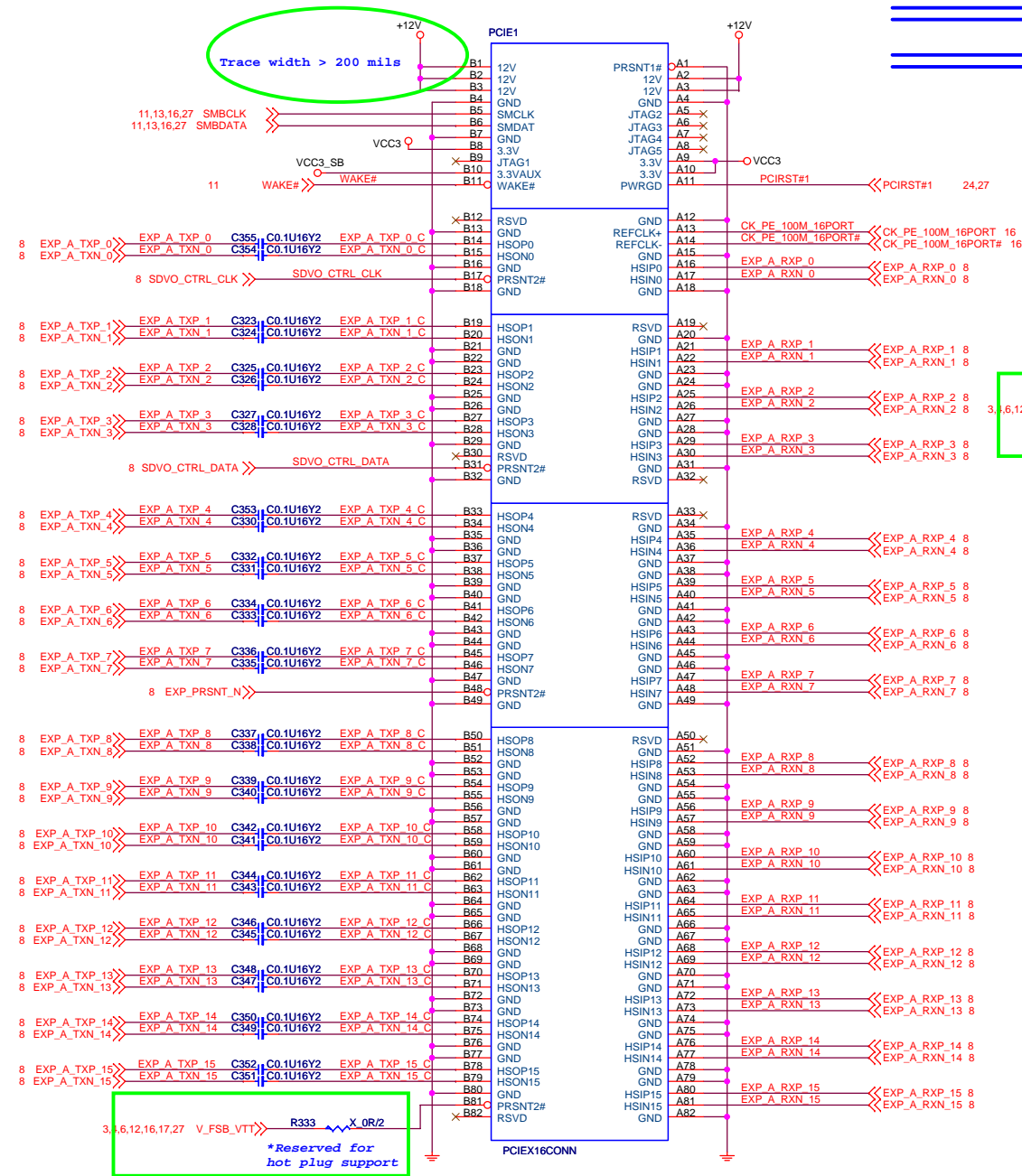
Document Description
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**Azalia CODEC(ALC888)**

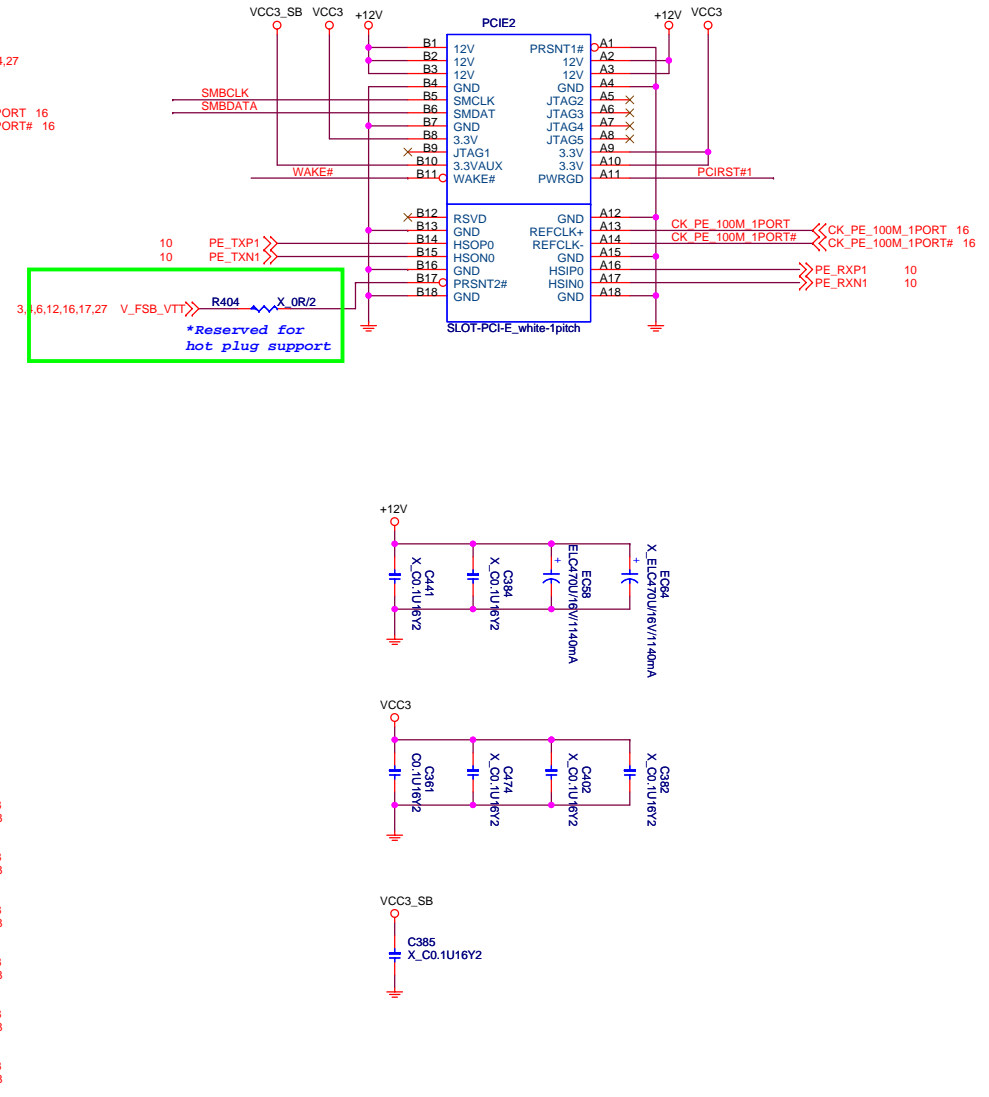
Rev  
20

Date: Tuesday, August 01, 2006 Sheet 21 of 36

# PCI EXPRESS 16-PORT



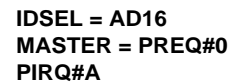
# PCI EXPRESS 1-PORT





10,26 AD[31..0] << AD[31..0]

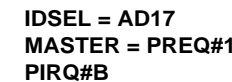
10,26 C\_BE#[3..0] << C\_BE#[3..0]



**PCI SLOT 2 (P**

-12V

PCI2



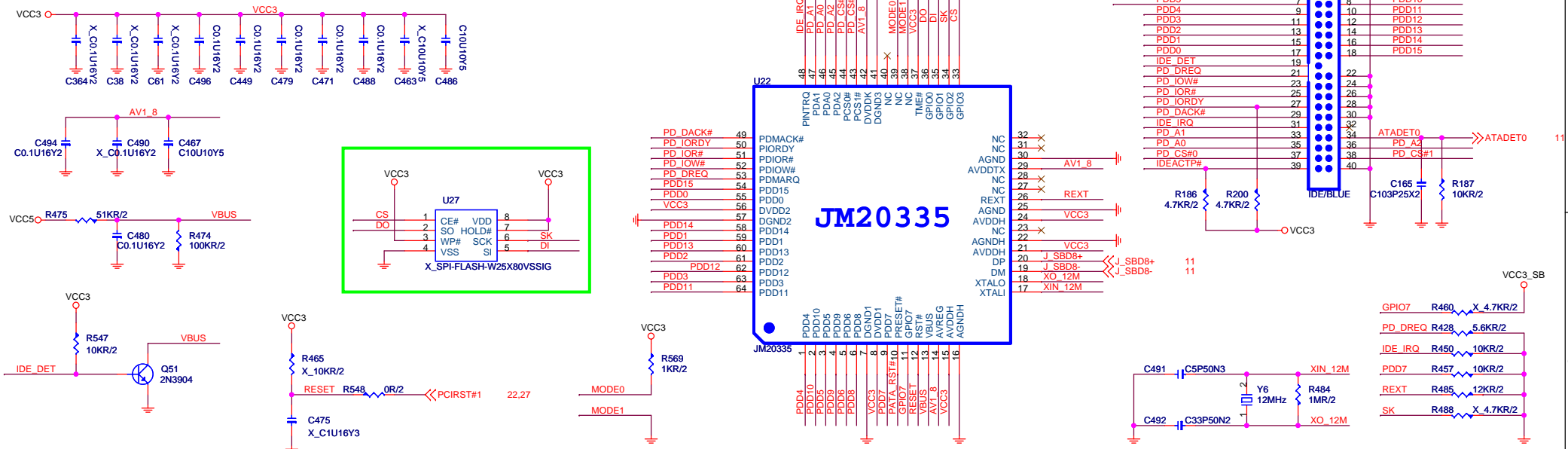
The diagram illustrates the timing for the 8P4R-4.7KR/2 module. It is divided into two sections: the top section for the 8P4R-8.2KR module and the bottom section for the 8P4R-4.7KR/2 module. Each section shows a sequence of signals (DEVSEL#, TRDY#, IRDY#, FRAME#, SERR#, PERR#, LOCK#, STOP#) and their corresponding timing relative to VCC3. The 8P4R-8.2KR module has a 10P8R-8.2KR module connected to it. The 8P4R-4.7KR/2 module has a 10P8R-2.7KR module connected to it. The signals are shown as red lines with blue and green markers indicating timing points. The 8P4R-8.2KR module has a 10P8R-8.2KR module connected to it. The 8P4R-4.7KR/2 module has a 10P8R-2.7KR module connected to it.



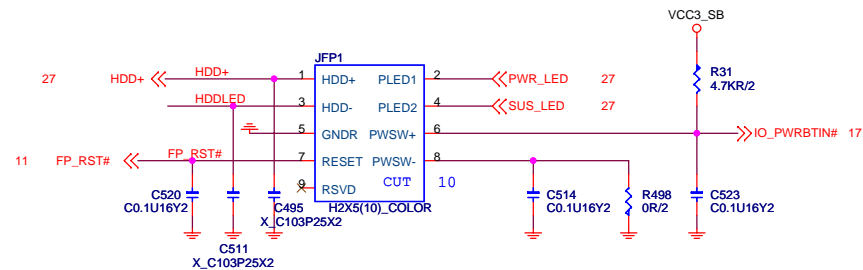
MS-7276

Size Custom	Document Description <b>PCI Slot 1 &amp; 2</b>	Rev 20
Date: Tuesday, August 01, 2006		Sheet 23 of 36

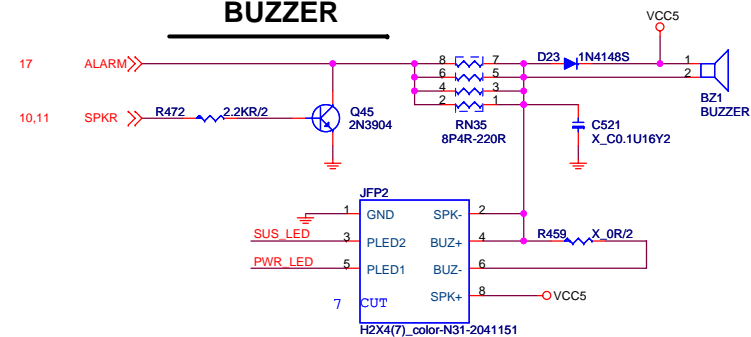
## Hi-Speed USB to PATA Bridge



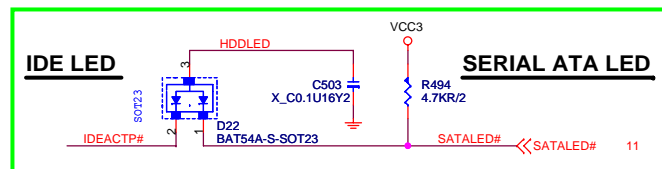
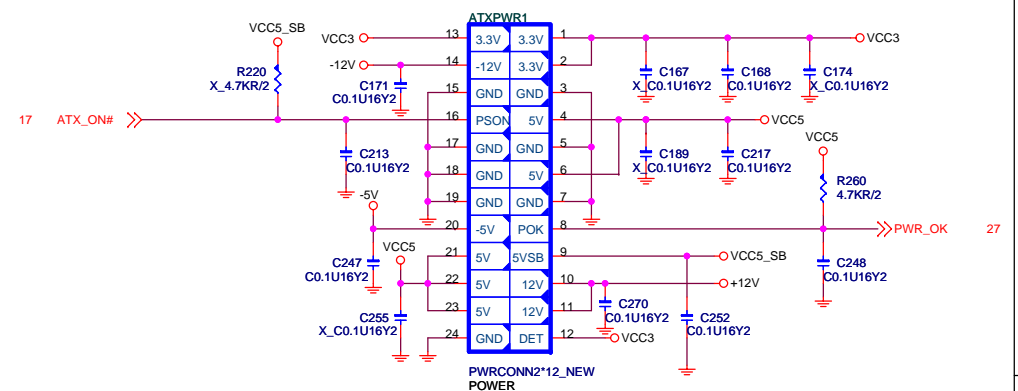
## Front Panel



**BUZZER**



## ATX CONNECTOR

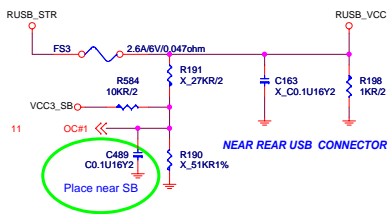


**MICRO-STAR INT'L CO.,LTD**

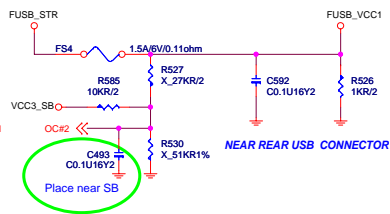
MS-7276

Size Custom	Document Description <b>ATX, IDE Connector &amp; F_Panel</b>	Rev 20
Date: Tuesday, August 01, 2006		Sheet 24 of 36

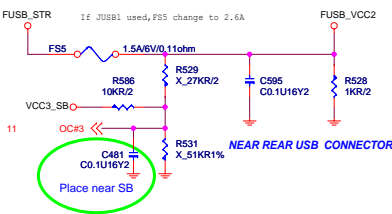
### POWER CIRCUIT FOR USB PORT 0,1,2,3



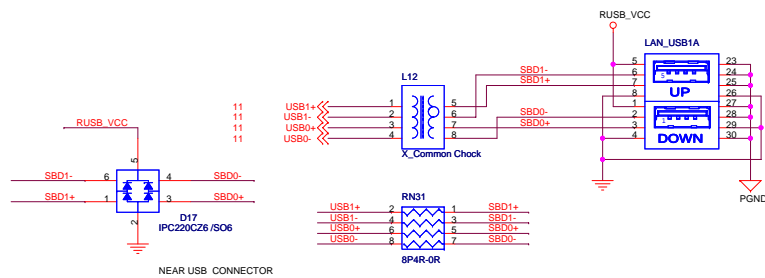
### POWER CIRCUIT FOR USB PORT 4,5



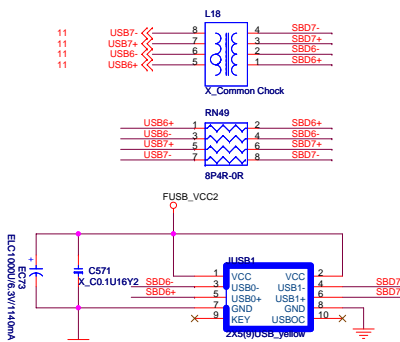
### POWER CIRCUIT FOR USB PORT 6,7



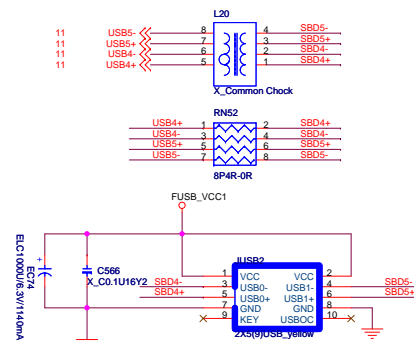
### REAR USB CONNECTOR FOR USB PORT 0,1



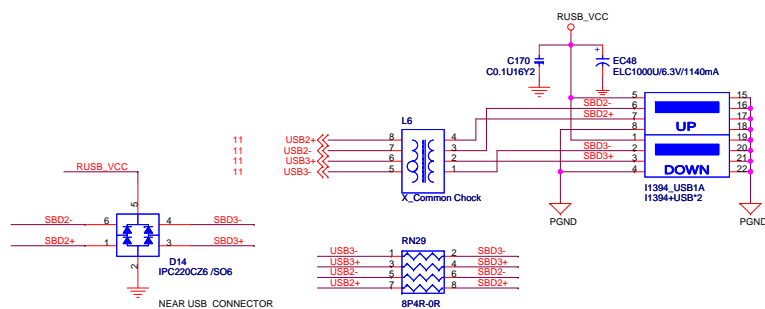
### FRONT USB CONNECTOR FOR USB PORT 6,7



### FRONT USB CONNECTOR FOR USB PORT 4,5

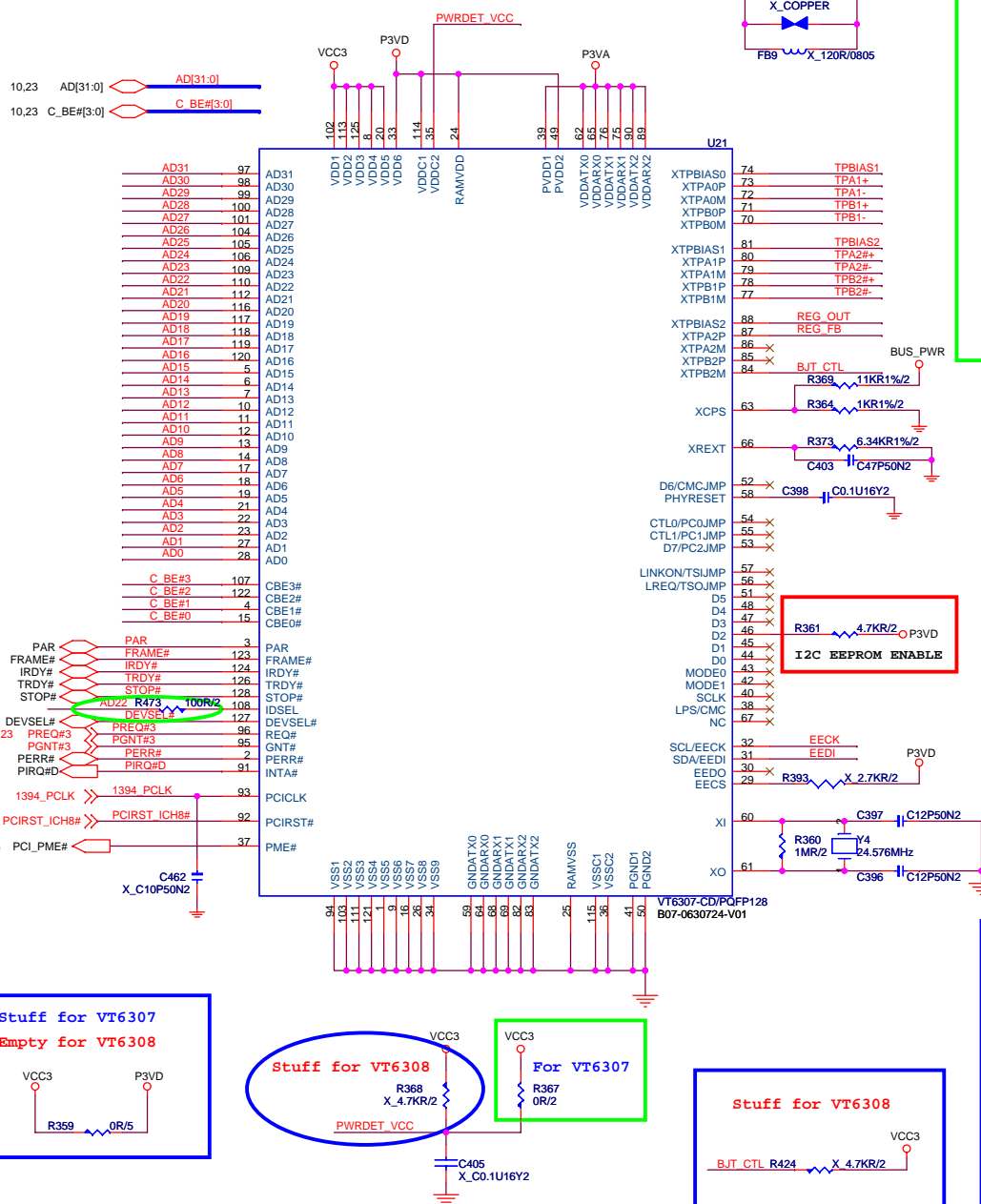
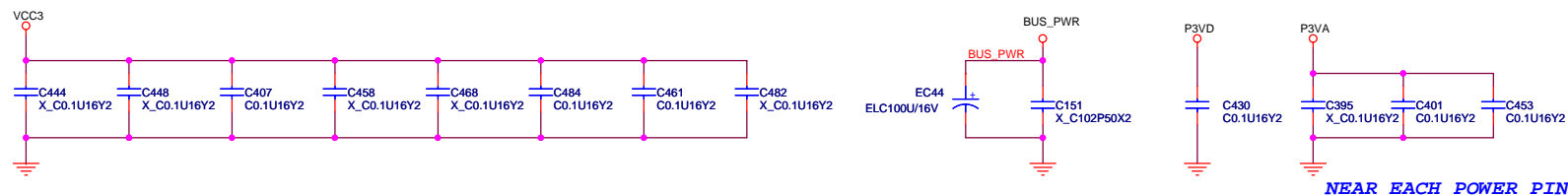


### REAR USB CONNECTOR FOR USB PORT 2,3

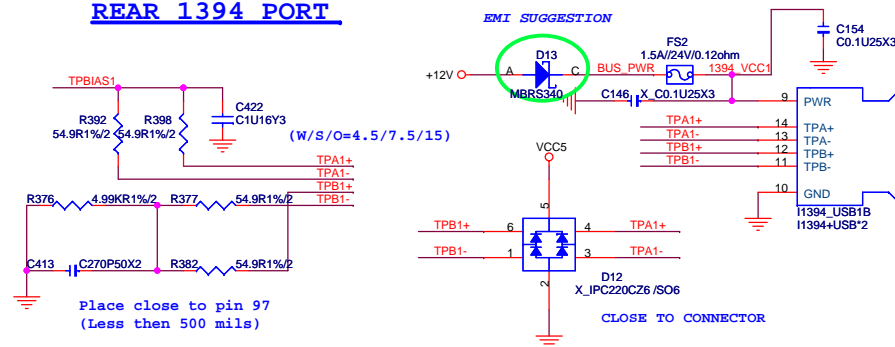


layout 蛭碓LJ PGND錫GND乙妻電 斬 ?50mil腔料蠟此穿

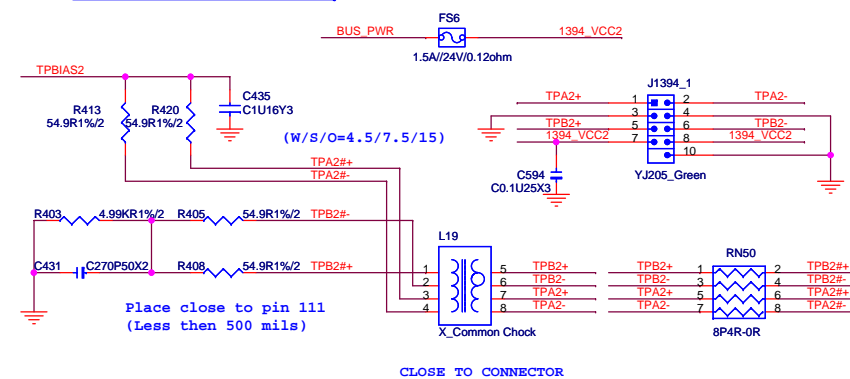
**IEEE-1394**



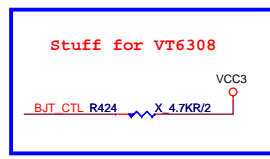
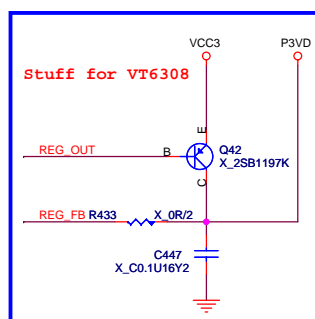
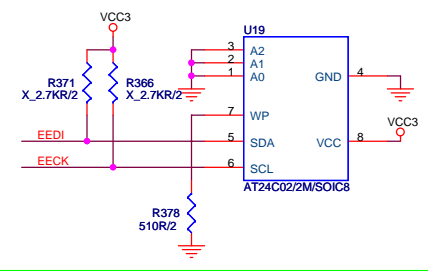
REAR 1394 PORT



FRONT 1394 PORT



1394-EEPROM 24C02



# ACPI Controller MS-7

## VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

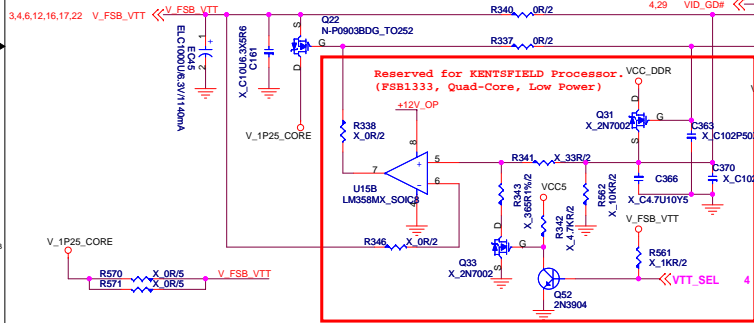
## 3VSB MODE SELECT

3VSB MODE	3VdLDEC
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

## DDR I & DDR II VOLT SELECT

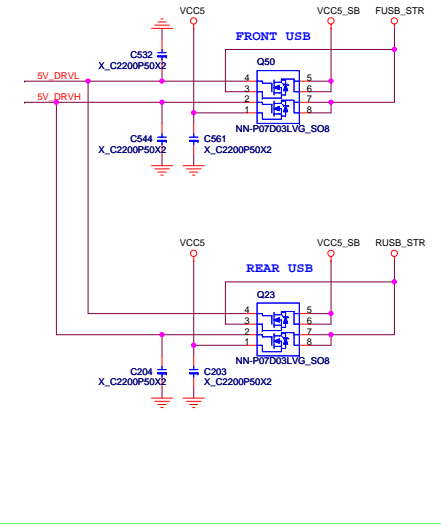
DDRTYPE	VdIMM
PULL LOW	2.5V
PULL HIGH	1.8V

## V\_FSB\_VTT 6.2A

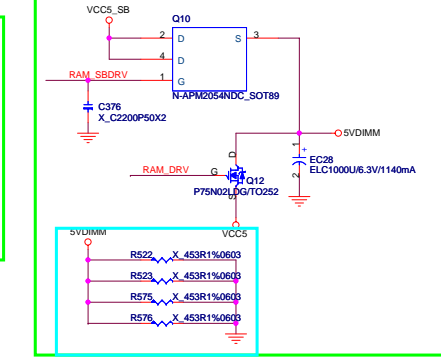


VTT_SEL = H	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = L	V_FSB_VTT=1.2V	For normal processors.

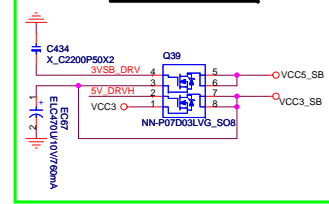
## 5V DUAL Power 5A



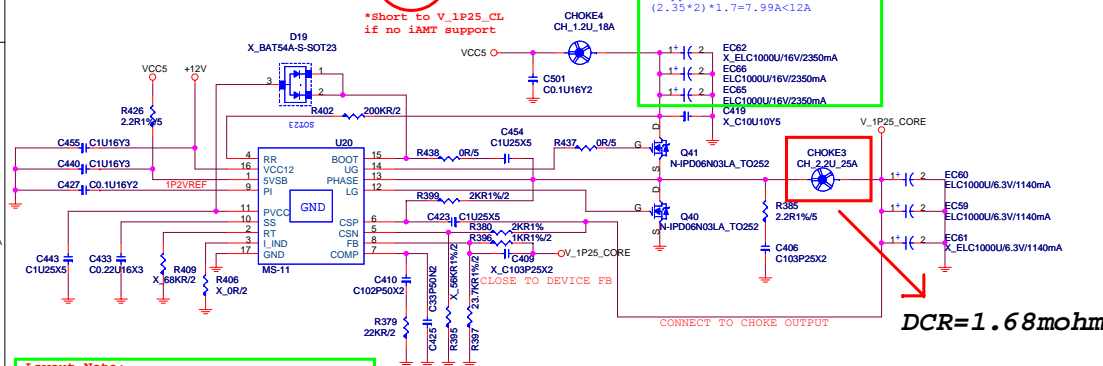
## 5VDIMM



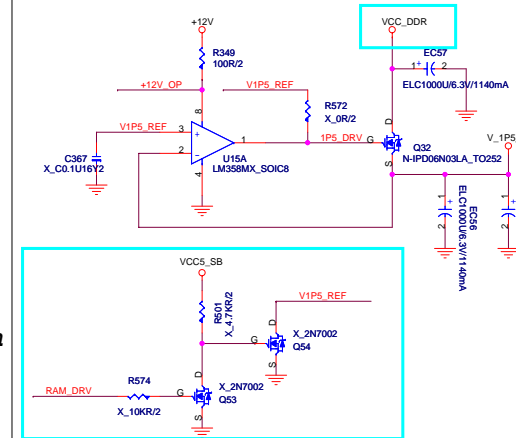
## VCC3\_SB Power



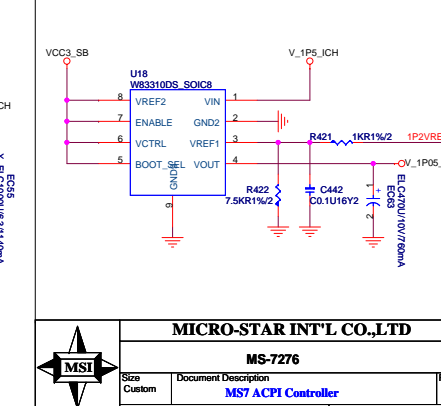
## V\_1P25\_CORE POWER...21.34A + 3.8A



## V\_1P5\_ICH...2A + 1.17A



## V\_1P05\_ICH...1.17A

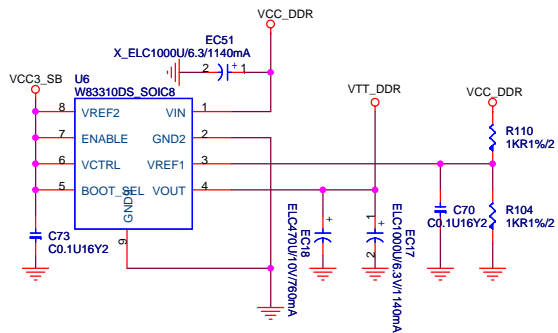


## MICRO-STAR INT'L CO.,LTD

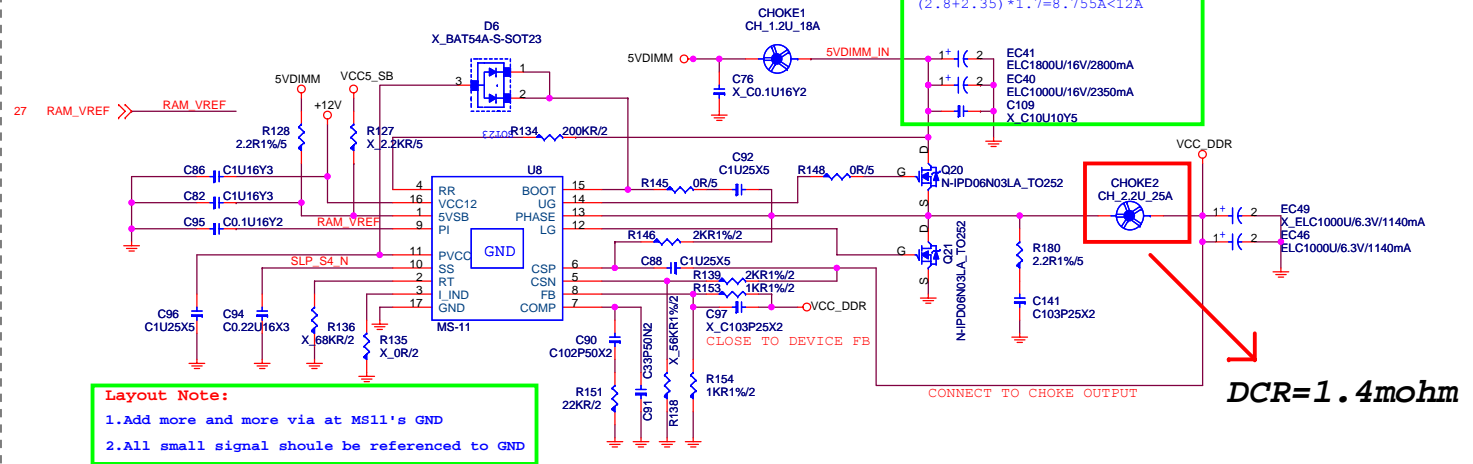
MS-7276

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## DDR II VTT POWER



## DDR II 1.8V POWER...25A



# Voltage Regular Module

N-P0903BDG\_TO252 mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V/25A), Vgs(on)=1~3V, Id=50A, Ciss=1800pf, Qg=50nC, Vds=25V, Vgs=±20V, RoHS COMPLIANCE

P75N02LDG/TO252 mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(10V, 30A), Vgs(on)=1~3V, Id=75A, Ciss=5000pf, Qg=140nC, Vds=25V, Vgs=±20V, RoHS COMPLIANCE

C100U2SP capacitor, 100uF, 2.5V, 105C, longlife change from 2000hrs to 3000hrs, KZJ series

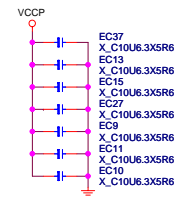
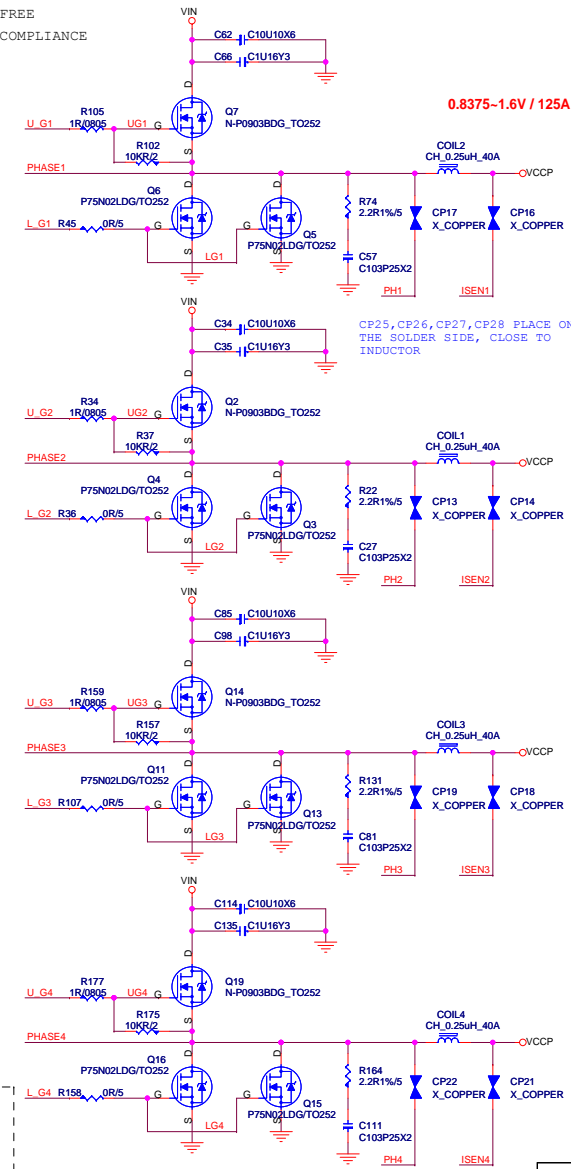
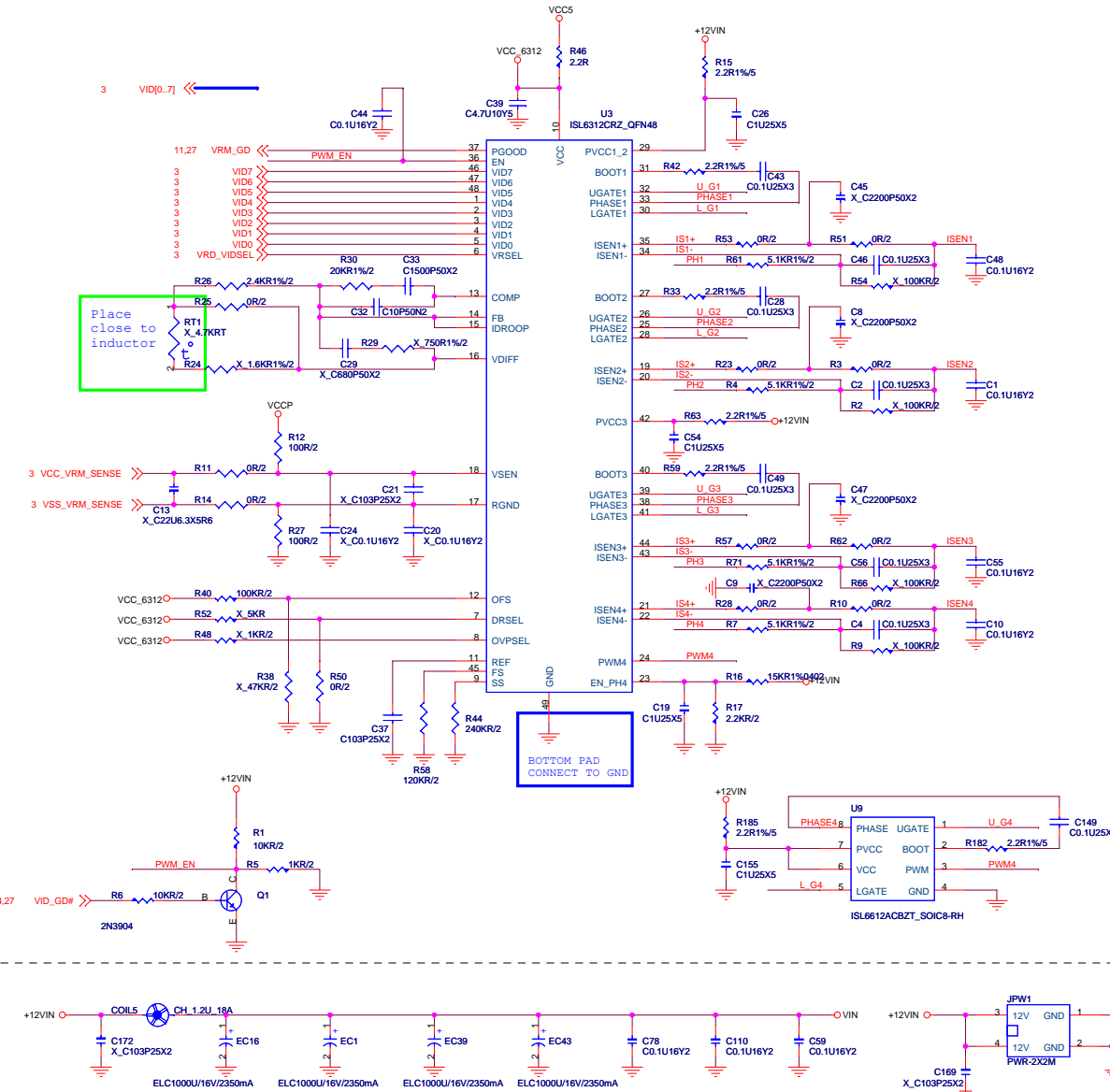
CD560U4OS-2 capacitor, 560uF, 4V, 105C, longlife change from 2000hrs to 3000hrs, KZJ series

1800UF/6.3V capacitor, 1800uF, 6.3V, 105C, longlife change from 2000hrs to 3000hrs, KZJ series

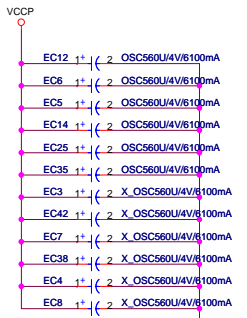
0.25uH/40A inductor, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mOhm, PEW, FERRITE, SQUARE, RoHS COMPLIANCE

CH-1.1U25A-LF inductor, 1.1uH, 20%, DIP/9mm, 25A, 1.4mOhm, 5.5T, 0.9mmx3, PEW, IRON, LEAD FREE

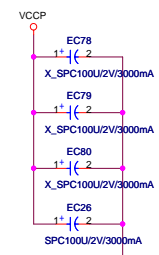
CD1000U16EL20-2 capacitor, 1000uF, 16V, Dip-8x20/3.5mm, 20%, 12mOhm, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE



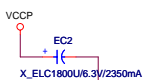
## OS-CON Capacitors



## SP Capacitors

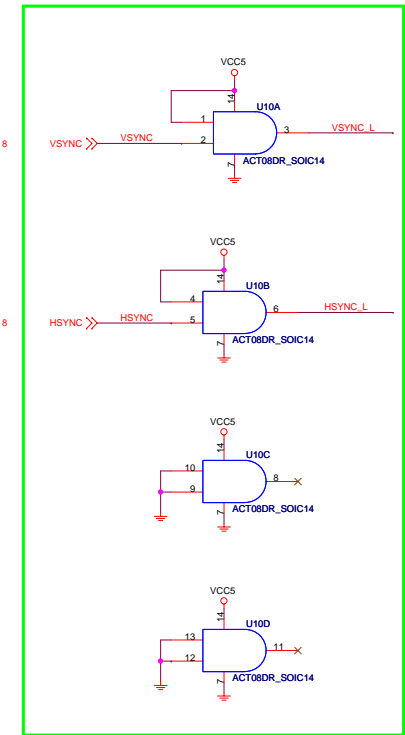
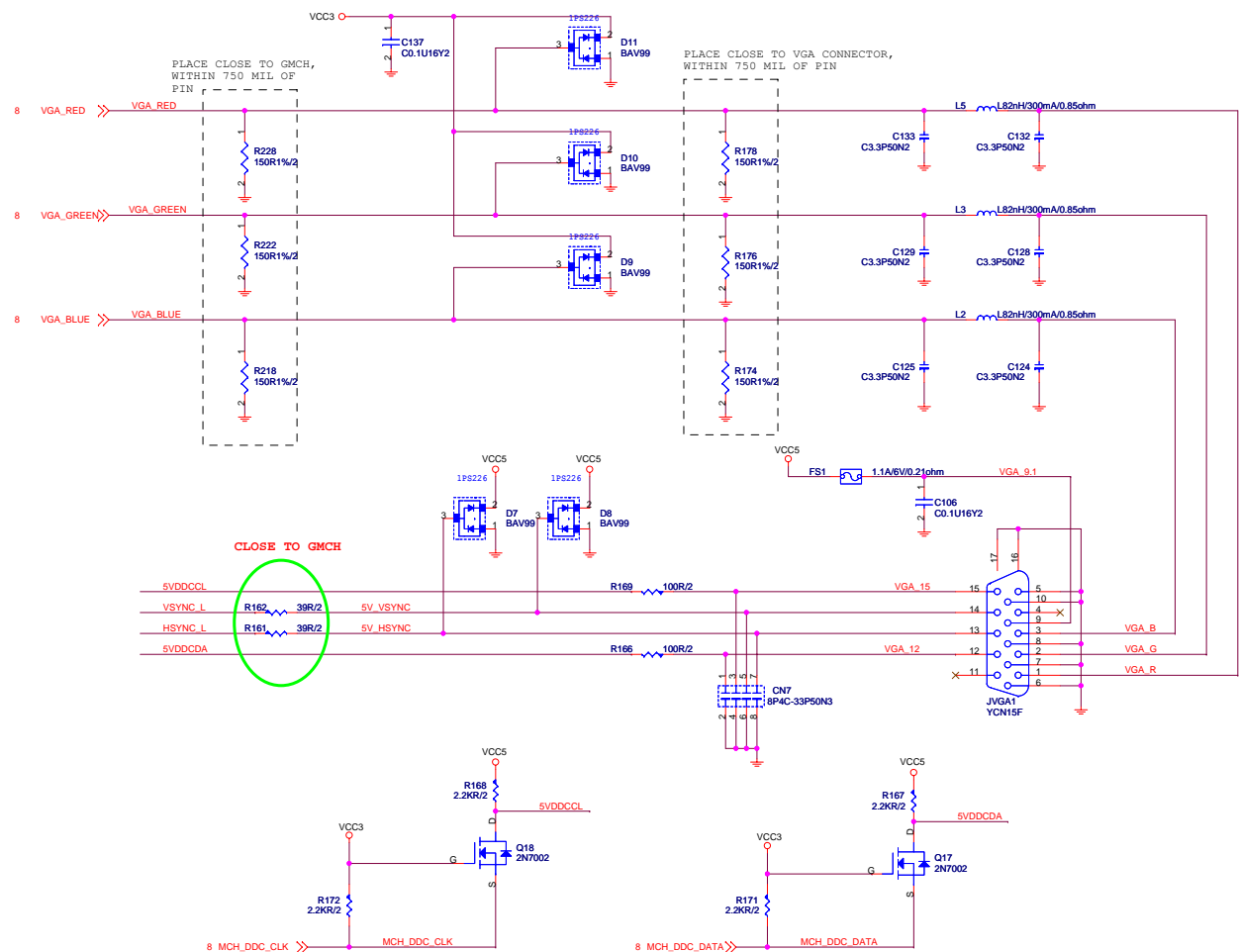


## EL Capacitors

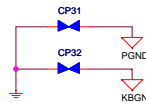
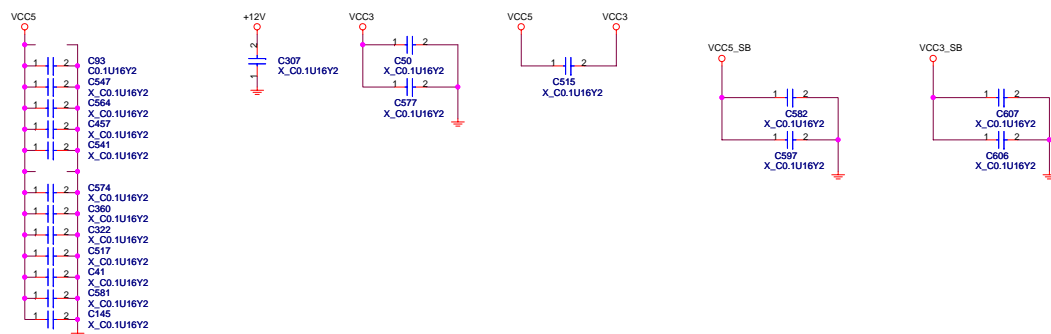




# Video Connector



## EMI Reserved



## ICH8

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO [7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO PME#
GPIO[9]	WOL EN		I/O	Resume	Y	Y	3.3V	Native	GPIO 9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO 10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO 14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO 19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO 21
GPIO[22]	SCLOCK		I/O	Core	Y		3.3V	GPI	GPIO 22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ 1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT IO#
GPIO[26]	S4 STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO 36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO 37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO 38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO 39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO 48
GPIO[49]	CPUPWRGD		I/O	V CPU IO			CPU	Native	H PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	REQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	REQ#1 PGNT#1	AD21	PCI_CLK2
1394	PIRQ#D	REQ#3 PGNT#3	AD22	1394_PCLK

## PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI_E X16 & PCI_E X1
PCIRST#2	SIO, 1394, FWH, TPM
PCIRST#3	PCI SLOT1&2,
PCIRST_ICH8#	MS7
HD_RST#	Primary IDE

## DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

## JUMPER SETTING

<b>JBAT1</b>	(1-2) NORMAL	(2-3) CLEAR
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0A modify 10 change list

- 1. Add R536 for SLP\_M
- 2. Q30.C connect to U8.10
- 3. change VTT\_DDR drived from VCC\_DDR
- 4. modify ALC883 circuit to meet the Vista "premium" SPEC
- 5. 1394 circuit modify, change net name from "VDD" to "P3VD" (page 26)
- 4. modify ALC883 circuit to meet the Vista "premium" SPEC
- 5. modify JM20335 circuit (page 24)
- 6. modify SMBLINK and SMBCLK/DATA circuit (page 11)
- 7. add C469 C539 for margin (page 12)
- 8. add R564 and R563 for ICS (page 16)
- 9. CPU FAN mornitor from AUXFANOUT change to CPUFANOUT1 (page 17)
- 10. add R566 and R567 for JM20335 (page 25)
- 11. modify V\_FSB\_VTT circuit (page 27)
- 12. change R51 R3 R62 R10 to 0ohm for power team solution (page 29)
- 13. modify V\_1P5\_ICH circuit from Vcc3 change to VCC\_DDR (page 27)
- 14. Add Q54 and Q53 for S3 sequence (page 27)
- 15. reserve R522 R523 R575 R576 蘇滅欄研?霜 (page 27)
- 16. add R578 R579 R580 R581 R582 R583 for 48M and 14M pull high and pull down (page 16)
- 17. Add C606 C607 for EMI (page 30)
- 18. Add R584 R585 R586 for option USB OC# function (page 25)
- 19. change C369 and C371 footprint to 0805 (page 20)

10 modify 20 change list

- 1. Add C608, C609, C610, C611 for ESD. (Page 10)
- 2. Add FB10, FB11 for passing Vista premium. (Page 21)
- 3. Delete JUSB3 circuit. (Page 25)